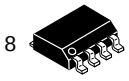
600 V / 4 A, High-Side Automotive Gate Driver IC

FAD7171MX



SOIC−8 NB
CASE 751−07

Description

The FAD7171MX is a monolithic high−side gate drive IC that can drive high−speed MOSFETs and IGBTs that operate up to +600 V. It has a buffered output stage with all NMOS transistors designed for high pulse current driving capability and minimum cross−conduction. **onsemi**'s high−voltage process and common−mode noise−canceling techniques provide stable operation of the high−side driver under high dv/dt noise circumstances. An advanced level−shift circuit offers high−side gate driver operation up to V_S = −11 V for VBS = 15 V.

The UVLO circuit prevents malfunction when VBS is lower than the specified threshold voltage. The high−current and low−output voltage−drop feature make this device suitable for sustaining switch drivers and energy−recovery switch drivers in automotive motor drive inverters, switching power supplies, and high−power DC−DC converter applications.

Features

- Floating Channel for Bootstrap Operation to +600 V
- 4 A Sourcing and 4 A Sinking Current Driving Capability
- Common−Mode dv/dt Noise−Cancelling Circuit
- 3.3 V and 5 V Input Logic Compatible
- Output In−phase with Input Signal
- Under−Voltage Lockout for V_{BS}
- 8−SOIC Package, Case 751−07 (JEDEC MS−012, 0.150 inch Narrow Body)
- AEC−Q100 Qualified and PPAP Capable for Ambient Operating Temperature from −40°C to 125°C

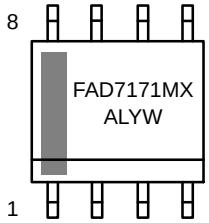
Applications

- Common Rail Injection Systems
- DC−DC Converter
- Motor Drive (Electric Power Steering, Fans)

Related Product Resources

- FAN7171 Product Folder
- FAD7171 Product Folder
- AND9674 Design and Application Guide of Bootstrap Circuit for High−Voltage Gate−Drive IC
- AN−8102 Recommendations to Avoid Short Pulse Width Issues in HVIC Gate Driver Applications
- AN−9052 Design Guide for Selection of Bootstrap Components

MARKING DIAGRAM



FAD717MX = Device
A = Assembly Site
L = Wafer Lot Number
YW = Assembly Start Week

ORDERING INFORMATION

Device	Package	Shipping†
FAD7171MX	SOIC8 (Pb−Free / Halogen Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

1. These devices passed wave soldering test by JESD22A−111.

TYPICAL APPLICATION

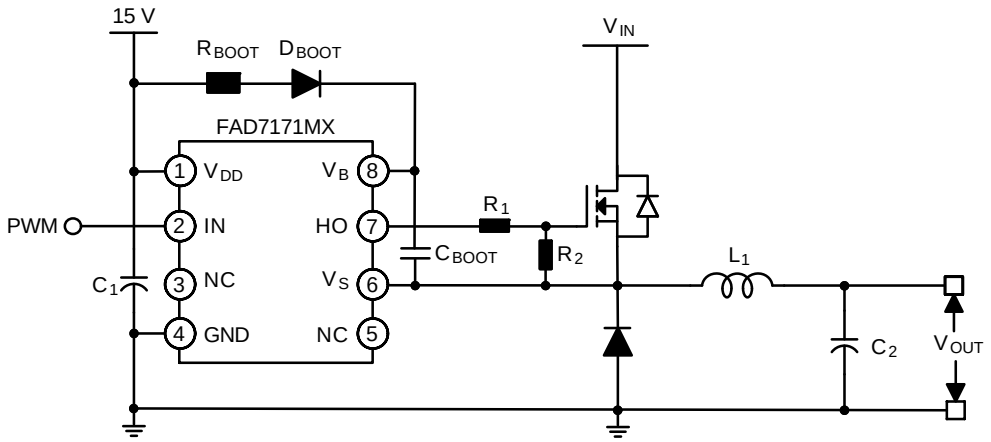


Figure 1. Typical Application

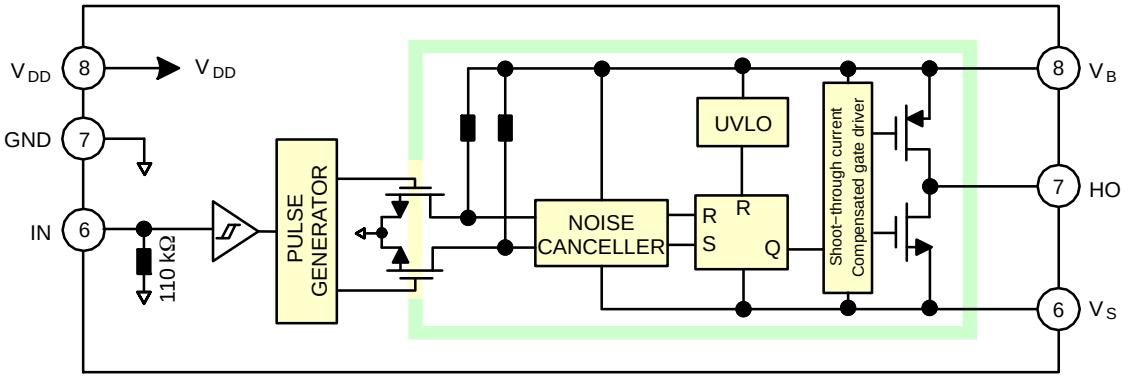


Figure 2. Block Diagram

PIN CONFIGURATION

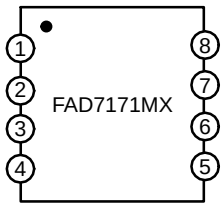


Figure 3. Pin Assignment (Top Through View)

PIN DESCRIPTION

Pin No.	Symbol	Description
1	V_{DD}	Supply Voltage
2	IN	Logic Input for High−Side Gate Driver Output
3	NC	No Connection
4	GND	Ground
5	NC	No Connection
6	V_S	High−Voltage Floating Supply Return
7	HO	High−Side Driver Output
8	V_B	High−Side Floating Supply

ABSOLUTE MAXIMUM RATINGS

Symbol	Characteristics	Min	Max	Unit
V_S	High−Side Floating Offset Voltage	V_B − 25	V_B + 0.3	V
V_B	High−Side Floating Supply Voltage	−0.3	625.0	V
V_{HO}	High−Side Floating Output Voltage	V_S − 0.3	V_B + 0.3	V
V_{DD}	Low−Side and Logic Supply Voltage	−0.3	25	V
V_{IN}	Logic Input Voltage	−0.3	V_{DD} + 0.3	V
dV_S/dt	Allowable Offset Voltage Slew Rate	−	±50	V/ns
P_D	Power Dissipation (Notes 2, 3, 4)	−	0.625	W
θ_{JA}	Thermal Resistance	−	200	°C/W
T_J	Junction Temperature	−55	150	°C
T_{STG}	Storage Temperature	−55	150	°C
T_A	Operating Ambient Temperature	−40	125	°C
ESD	Human Body Model (HBM)	−	2000	V
	Charge Device Model (CDM)	−	500	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Mounted on 76.2 x 114.3 x 1.6 mm PCB (FR−4 glass epoxy material).
3. Refer to the following standards:
   JESD51−2: Integral circuits thermal test method environmental conditions, natural convection, and
   JESD51−3: Low effective thermal conductivity test board for leaded surface−mount packages.
4. Do not exceed power dissipation (P_D) under any circumstances.

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Unit
V_{BS}	High−Side Floating Supply Voltage	10	20	V
V_S	High−Side Floating Supply Offset Voltage (DC) @ VBS = 15 V	−11	600	V
V_{HO}	High−Side Output Voltage	V_S	V_B	V
V_{IN}	Logic Input Voltage	GND	V_{DD}	V
V_{DD}	Supply Voltage	10	20	V
T_{PULSE}	Minimum Input Pulse Width	80	−	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (V_{BIAS} (V_{DD}, V_{BS}) = 15 V, −40°C ≤ T_A ≤ 125°C, unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to GND. The V_O and I_O parameters are relative to V_S and are applicable to the respective output HO)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
POWER SUPPLY SECTION						
I_{QDD}	Quiescent V_{DD} Supply Current	V_{IN} = 0 V or 5 V	−	85	200	μA
I_{PDD}	Operating V_{DD} Supply Current	C_{LOAD} = 1 nF, f_{IN} = 20 kHz	−	105	170	μA
BOOTSTRAPPED SUPPLY SECTION						
V_{BSUV+}	V_{BS} Supply Under−Voltage Positive−Going Threshold Voltage	V_{BS} = Sweep	8.4	9.4	10.1	V
V_{BSUV-}	V_{BS} Supply Under−Voltage Negative−Going Threshold Voltage	V_{BS} = Sweep	7.7	8.7	9.3	V
V_{BSHYS}	V_{BS} Supply UVLO Hysteresis Voltage	V_{BS} = Sweep	−	0.7	−	V
I_{LK}	Offset Supply Leakage Current	V_B = V_S = 600 V	−	−	50	μA
I_{QBS}	Quiescent V_{BS} Supply Current	V_{IN} = 0 V or 5 V	−	43	95	μA
I_{PBS}	Operating V_{BS} Supply Current	C_{LOAD} = 1 nF, f_{IN} = 20 kHz	−	620	1200	μA
INPUT LOGIC SECTION (IN)						
V_{IH}	Logic “1” Input Voltage		1.8	−	−	V
V_{IL}	Logic “0” Input Voltage			−	0.8	V
V_{INHYS}	Logic Input Hysteresis Voltage		−	0.5	−	V
I_{IN+}	Logic Input High Bias Current	V_{IN} = 5 V	−	45	100	μA
I_{IN-}	Logic Input Low Bias Current	V_{IN} = 0 V	−	−	2	μA
R_{IN}	Input Pull−down Resistance		30	105	−	kΩ
GATE DRIVER OUTPUT SECTION (HO)						
V_{OH}	High Level Output Voltage (V_{BIAS} − V_O)	No Load	−	−	35	mV
V_{OL}	Low Level Output Voltage	No Load	−	−	35	mV
I_{O+}	Output High, Short−Circuit Pulsed Current (Note 5)	V_{HO} = 0 V, V_{IN} = 5 V, PW ≤ 10 μs	2.5	4.0	−	A
I_{O-}	Output Low, Short−Circuit Pulsed Current (Note 5)	V_{HO} = 15 V, V_{IN} = 0 V, PW ≤ 10 μs	2.5	4.0	−	A
V_S	Allowable Negative V_S Pin Voltage for IN Signal Propagation to HO		−	−	11	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. These parameters guaranteed by design.

DYNAMIC ELECTRICAL CHARACTERISTICS (V_{BIAS} (V_{DD}, V_{BS}) = 15 V, V_S = GND = 0 V, C_L =1000 pF, and −40°C ≤ T_A ≤ 125°C, unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{ON}	Turn−On Propagation Delay	V_S = 0 V	−	48	100	ns
t_{OFF}	Turn−Off Propagation Delay	V_S = 0 V	−	46	95	ns
t_R	Turn−On Rise Time		−	11	18	ns
t_F	Turn−Off Fall Time		−	12	19	ns

TYPICAL PERFORMANCE CHARACTERISTICS

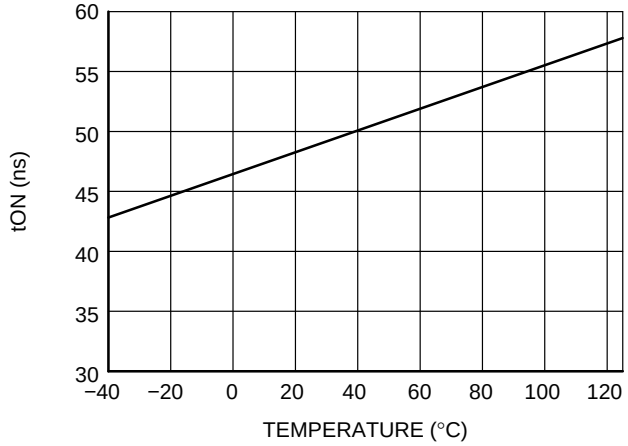


Figure 4. Turn−On Propagation Delay vs. Temperature

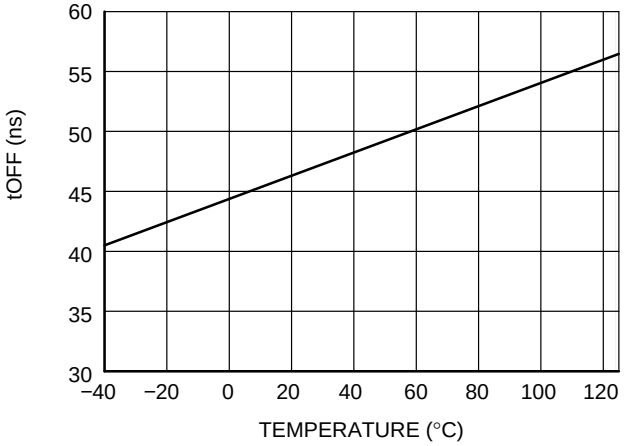


Figure 5. Turn−Off Propagation Delay vs. Temperature

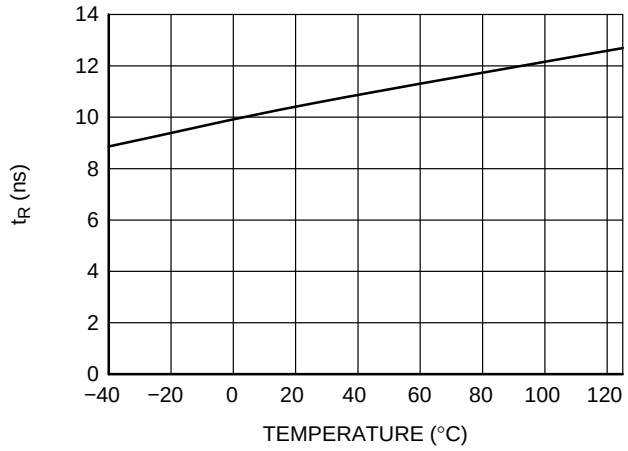


Figure 6. Turn−On Rise Time vs. Temperature

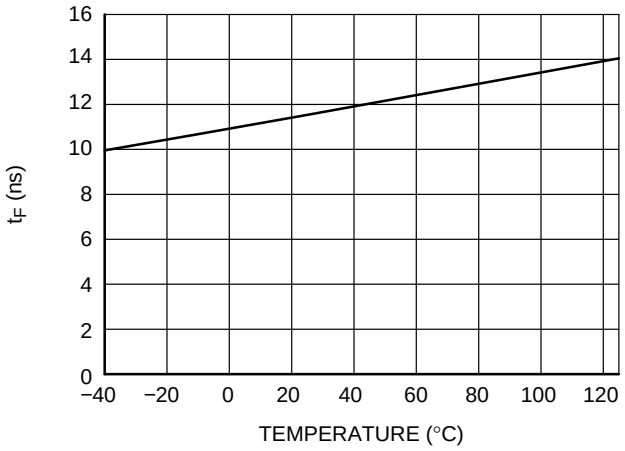


Figure 7. Turn−Off Fall Time vs. Temperature

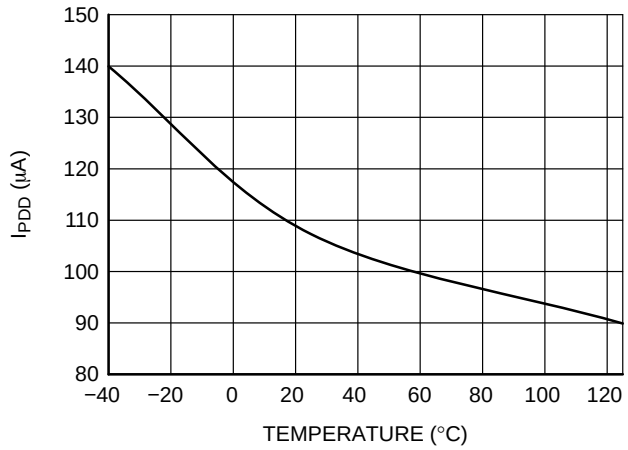


Figure 8. Operating V_{DD} Supply Current vs. Temperature

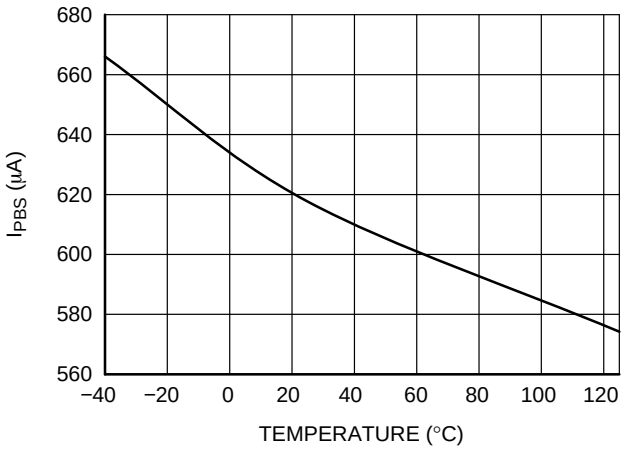


Figure 9. Operating V_{BS} Supply Current vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

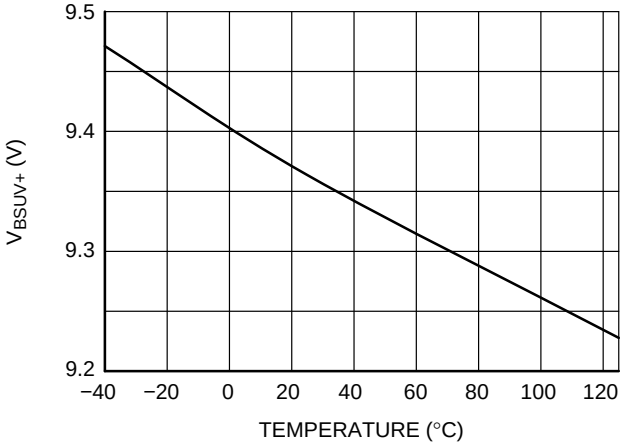


Figure 10. V_{BS} UVLO+ vs. Temperature

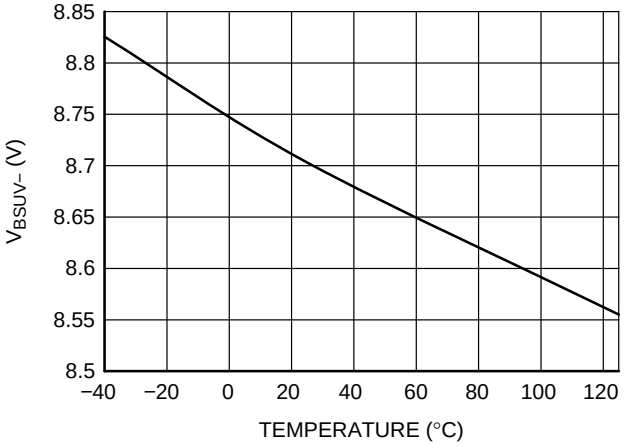


Figure 11. V_{BS} UVLO− vs. Temperature

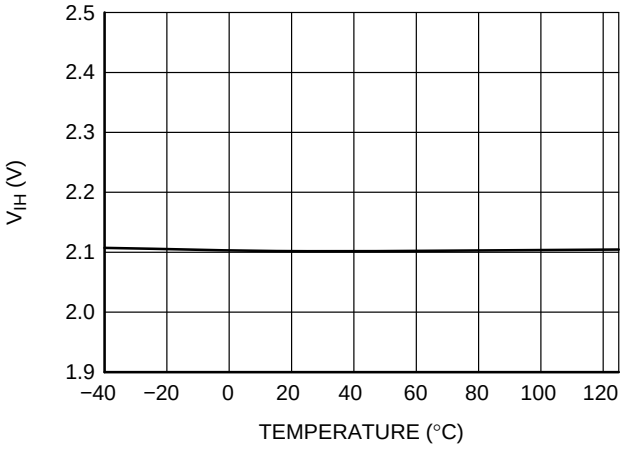


Figure 12. Logic High Input Voltage vs. Temperature

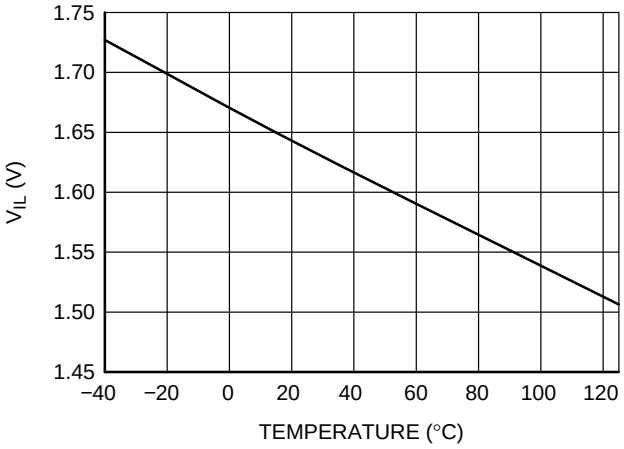


Figure 13. Logic Low Input Voltage vs. Temperature

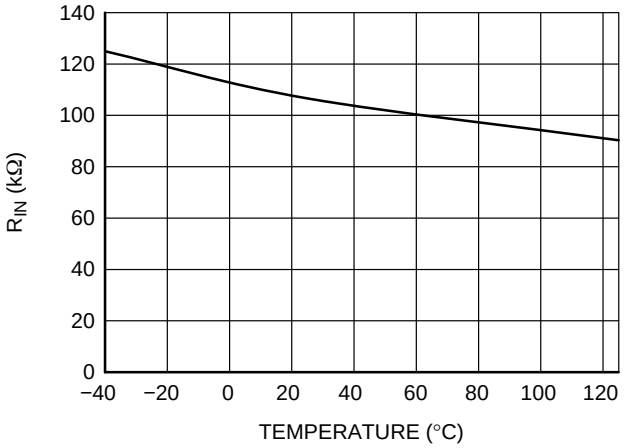


Figure 14. RIN vs. Temperature

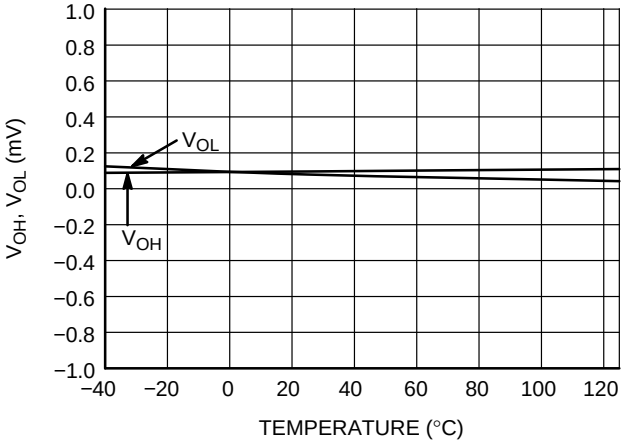


Figure 15. Output Voltage vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

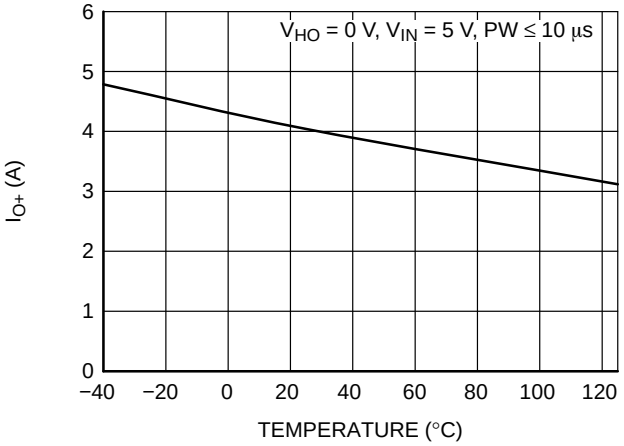


Figure 16. Output High, Short−Circuit Pulsed Current vs. Temperature

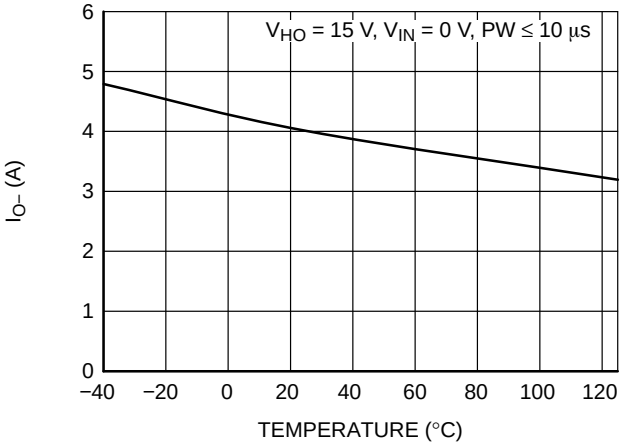


Figure 17. Output Low, Short−Circuit Pulsed Current vs. Temperature

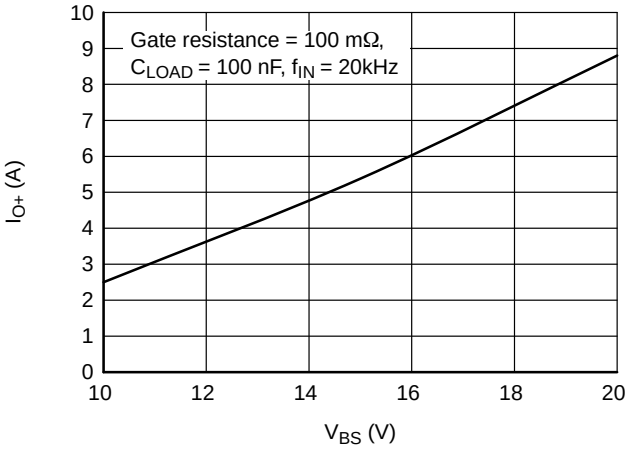


Figure 18. Output High, Short−Circuit Pulsed Current vs. Supply Voltage

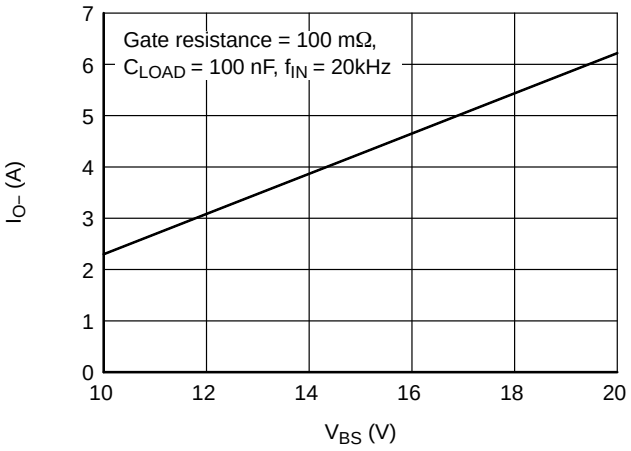


Figure 19. Output Low, Short−Circuit Pulsed Current vs. Supply Voltage

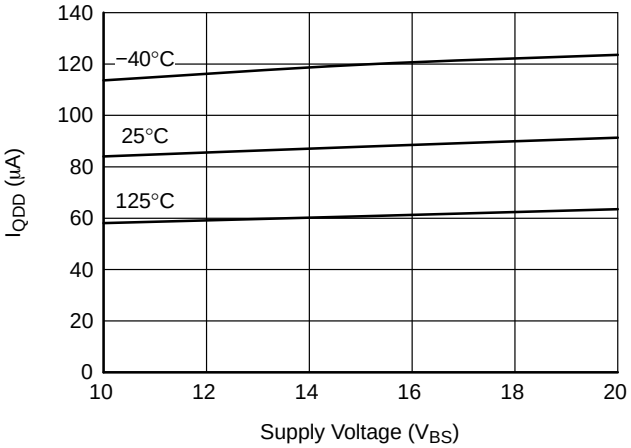


Figure 21. Quiescent V_{DD} Supply Current vs. Supply Voltage

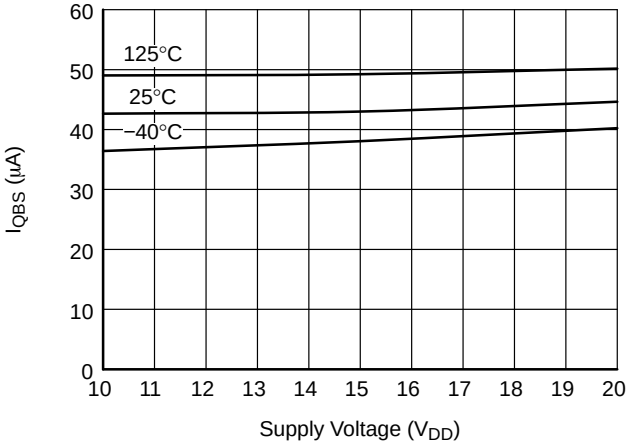


Figure 20. Quiescent V_{BS} Supply Current vs. Supply Voltage

SWITCHING TIME DEFINITIONS

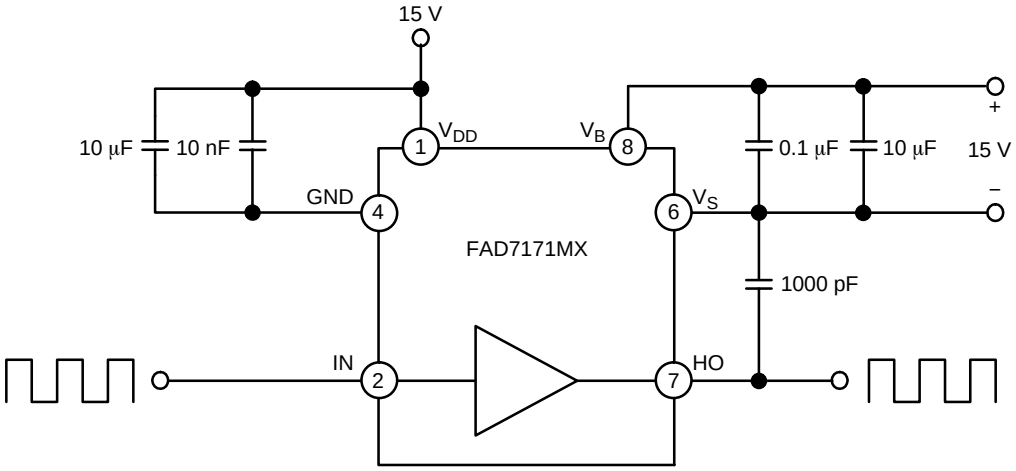


Figure 22. Switching Time Test Circuit (Referenced 8−SOIC)

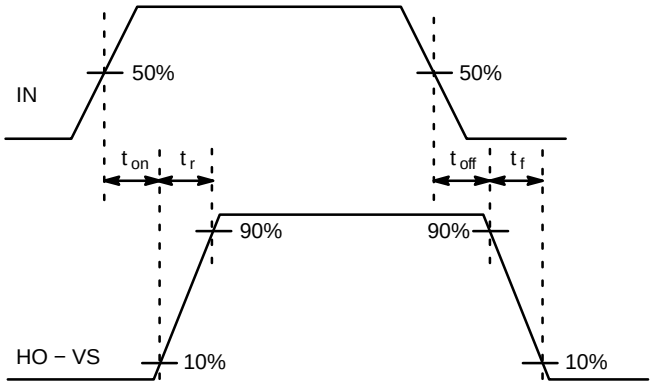
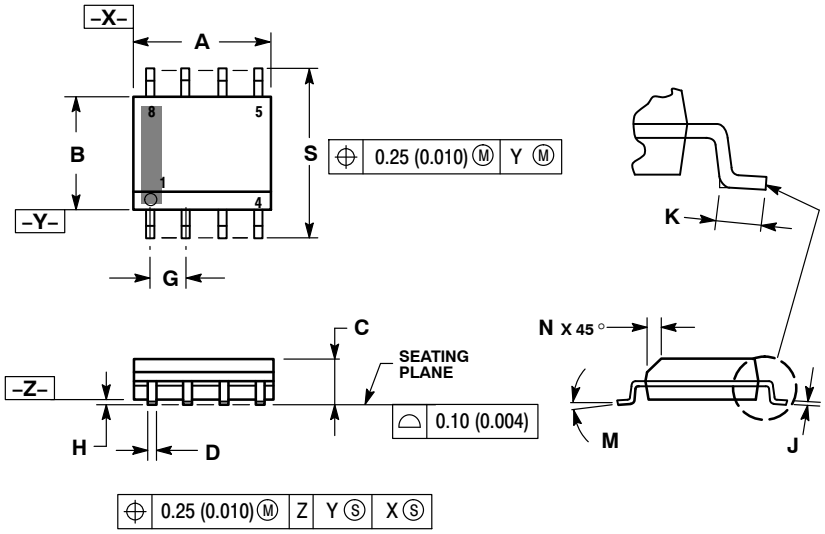


Figure 23. Switching Time Waveform Definitions

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

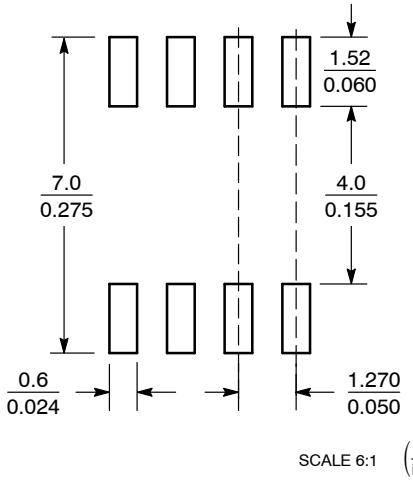
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

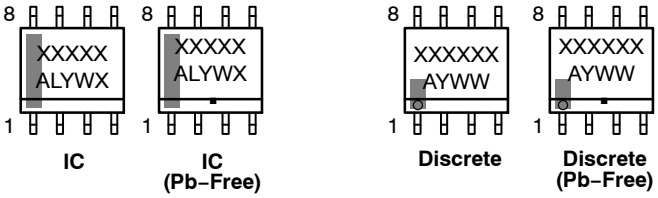
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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