

# 600 V / 4 A, High-Side Automotive Gate Driver IC

## FAD7171MX



### Description

The FAD7171MX is a monolithic high-side gate drive IC that can drive high-speed MOSFETs and IGBTs that operate up to +600 V. It has a buffered output stage with all NMOS transistors designed for high pulse current driving capability and minimum cross-conduction. onsemi's high-voltage process and common-mode noise-canceling techniques provide stable operation of the high-side driver under high dv/dt noise circumstances. An advanced level-shift circuit offers high-side gate driver operation up to  $V_S = -11$  V for  $V_{BS} = 15$  V.

The UVLO circuit prevents malfunction when  $V_{BS}$  is lower than the specified threshold voltage. The high-current and low-output voltage-drop feature make this device suitable for sustaining switch drivers and energy-recovery switch drivers in automotive motor drive inverters, switching power supplies, and high-power DC-DC converter applications.

### Features

- Floating Channel for Bootstrap Operation to +600 V
- 4 A Sourcing and 4 A Sinking Current Driving Capability
- Common-Mode dv/dt Noise-Cancelling Circuit
- 3.3 V and 5 V Input Logic Compatible
- Output In-phase with Input Signal
- Under-Voltage Lockout for  $V_{BS}$
- 8-SOIC Package, Case 751-07 (JEDEC MS-012, 0.150 inch Narrow Body)
- AEC-Q100 Qualified and PPAP Capable for Ambient Operating Temperature from -40°C to 125°C

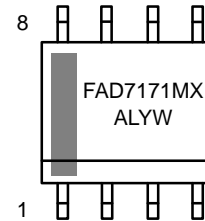
### Applications

- Common Rail Injection Systems
- DC-DC Converter
- Motor Drive (Electric Power Steering, Fans)

### Related Product Resources

- [FAN7171 Product Folder](#)
- [FAD7171 Product Folder](#)
- [AND9674](#) Design and Application Guide of Bootstrap Circuit for High-Voltage Gate-Drive IC
- [AN-8102](#) Recommendations to Avoid Short Pulse Width Issues in HVIC Gate Driver Applications
- [AN-9052](#) Design Guide for Selection of Bootstrap Components

### MARKING DIAGRAM



FAD7171MX = Device  
 A = Assembly Site  
 L = Wafer Lot Number  
 YW = Assembly Start Week

### ORDERING INFORMATION

Device	Package	Shipping†
FAD7171MX	SOIC8 (Pb-Free / Halogen Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

1. These devices passed wave soldering test by JESD22A-111.

# FAD7171MX

## TYPICAL APPLICATION

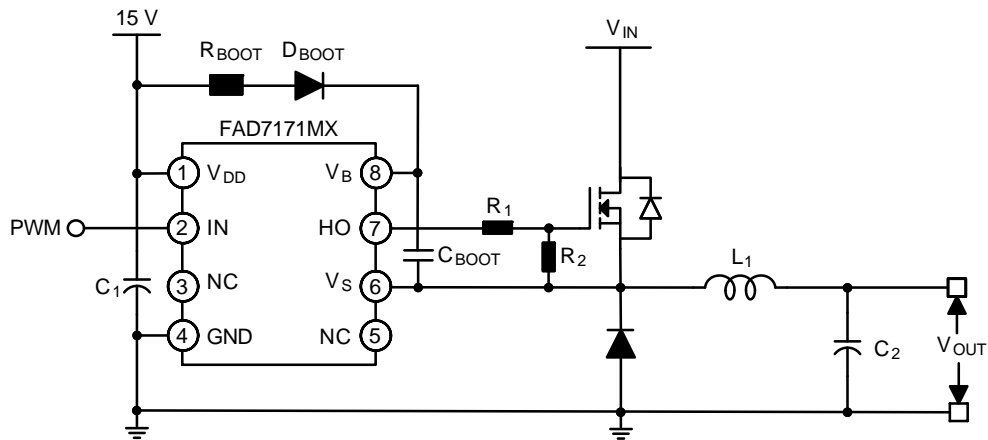


Figure 1. Typical Application

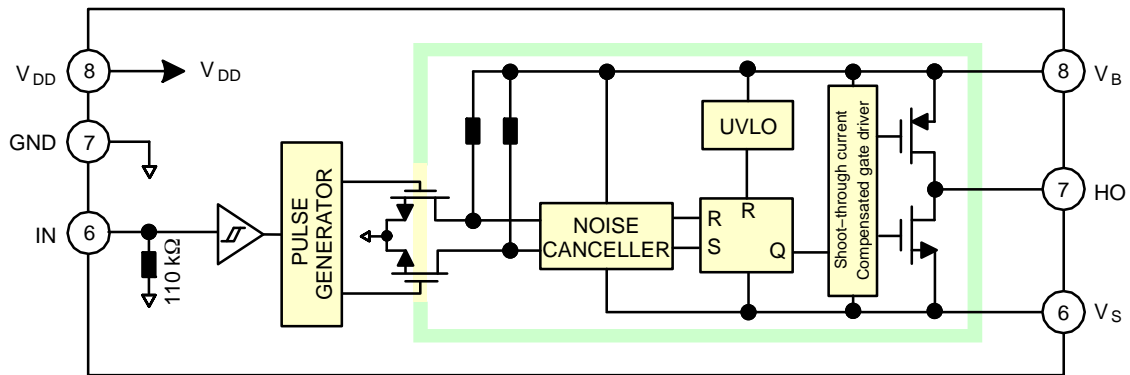


Figure 2. Block Diagram

## PIN CONFIGURATION

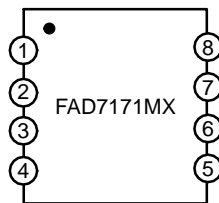


Figure 3. Pin Assignment (Top Through View)

# FAD7171MX

## PIN DESCRIPTION

Pin No.	Symbol	Description
1	V <sub>DD</sub>	Supply Voltage
2	IN	Logic Input for High-Side Gate Driver Output
3	NC	No Connection
4	GND	Ground
5	NC	No Connection
6	V <sub>S</sub>	High-Voltage Floating Supply Return
7	HO	High-Side Driver Output
8	V <sub>B</sub>	High-Side Floating Supply

## ABSOLUTE MAXIMUM RATINGS

Symbol	Characteristics	Min	Max	Unit
V <sub>S</sub>	High-Side Floating Offset Voltage	V <sub>B</sub> - 25	V <sub>B</sub> + 0.3	V
V <sub>B</sub>	High-Side Floating Supply Voltage	-0.3	625.0	V
V <sub>HO</sub>	High-Side Floating Output Voltage	V <sub>S</sub> - 0.3	V <sub>B</sub> + 0.3	V
V <sub>DD</sub>	Low-Side and Logic Supply Voltage	-0.3	25	V
V <sub>IN</sub>	Logic Input Voltage	-0.3	V <sub>DD</sub> + 0.3	V
dV <sub>S</sub> /dt	Allowable Offset Voltage Slew Rate	-	±50	V/ns
P <sub>D</sub>	Power Dissipation (Notes 2, 3, 4)	-	0.625	W
θ <sub>JA</sub>	Thermal Resistance	-	200	°C/W
T <sub>J</sub>	Junction Temperature	-55	150	°C
T <sub>STG</sub>	Storage Temperature	-55	150	°C
T <sub>A</sub>	Operating Ambient Temperature	-40	125	°C
ESD	Human Body Model (HBM)	-	2000	V
	Charge Device Model (CDM)	-	500	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Mounted on 76.2 x 114.3 x 1.6 mm PCB (FR-4 glass epoxy material).

3. Refer to the following standards:

JESD51-2: Integral circuits thermal test method environmental conditions, natural convection, and

JESD51-3: Low effective thermal conductivity test board for leaded surface-mount packages.

4. Do not exceed power dissipation (P<sub>D</sub>) under any circumstances.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Unit
V <sub>BS</sub>	High-Side Floating Supply Voltage	10	20	V
V <sub>S</sub>	High-Side Floating Supply Offset Voltage (DC) @ V <sub>BS</sub> = 15 V	-11	600	V
V <sub>HO</sub>	High-Side Output Voltage	V <sub>S</sub>	V <sub>B</sub>	V
V <sub>IN</sub>	Logic Input Voltage	GND	V <sub>DD</sub>	V
V <sub>DD</sub>	Supply Voltage	10	20	V
T <sub>PULSE</sub>	Minimum Input Pulse Width	80	-	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

# FAD7171MX

**ELECTRICAL CHARACTERISTICS** ( $V_{BIAS}$  ( $V_{DD}$ ,  $V_{BS}$ ) = 15 V,  $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ , unless otherwise specified. The  $V_{IN}$  and  $I_{IN}$  parameters are referenced to GND. The  $V_O$  and  $I_O$  parameters are relative to  $V_S$  and are applicable to the respective output HO)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
--------	-----------	------------	-----	-----	-----	------

## POWER SUPPLY SECTION

$I_{QDD}$	Quiescent $V_{DD}$ Supply Current	$V_{IN} = 0 \text{ V or } 5 \text{ V}$	–	85	200	$\mu\text{A}$
$I_{PDD}$	Operating $V_{DD}$ Supply Current	$C_{LOAD} = 1 \text{ nF}$ , $f_{IN} = 20 \text{ kHz}$	–	105	170	$\mu\text{A}$

## BOOTSTRAPPED SUPPLY SECTION

$V_{BSUV+}$	$V_{BS}$ Supply Under-Voltage Positive-Going Threshold Voltage	$V_{BS} = \text{Sweep}$	8.4	9.4	10.1	V
$V_{BSUV-}$	$V_{BS}$ Supply Under-Voltage Negative-Going Threshold Voltage	$V_{BS} = \text{Sweep}$	7.7	8.7	9.3	V
$V_{BSHYS}$	$V_{BS}$ Supply UVLO Hysteresis Voltage	$V_{BS} = \text{Sweep}$	–	0.7	–	V
$I_{LK}$	Offset Supply Leakage Current	$V_B = V_S = 600 \text{ V}$	–	–	50	$\mu\text{A}$
$I_{QBS}$	Quiescent $V_{BS}$ Supply Current	$V_{IN} = 0 \text{ V or } 5 \text{ V}$	–	43	95	$\mu\text{A}$
$I_{PBS}$	Operating $V_{BS}$ Supply Current	$C_{LOAD} = 1 \text{ nF}$ , $f_{IN} = 20 \text{ kHz}$	–	620	1200	$\mu\text{A}$

## INPUT LOGIC SECTION (IN)

$V_{IH}$	Logic "1" Input Voltage		1.8	–	–	V
$V_{IL}$	Logic "0" Input Voltage			–	0.8	V
$V_{INHYS}$	Logic Input Hysteresis Voltage		–	0.5	–	V
$I_{IN+}$	Logic Input High Bias Current	$V_{IN} = 5 \text{ V}$	–	45	100	$\mu\text{A}$
$I_{IN-}$	Logic Input Low Bias Current	$V_{IN} = 0 \text{ V}$	–	–	2	$\mu\text{A}$
$R_{IN}$	Input Pull-down Resistance		30	105	–	$\text{k}\Omega$

## GATE DRIVER OUTPUT SECTION (HO)

$V_{OH}$	High Level Output Voltage ( $V_{BIAS} - V_O$ )	No Load	–	–	35	mV
$V_{OL}$	Low Level Output Voltage	No Load	–	–	35	mV
$I_{O+}$	Output High, Short-Circuit Pulsed Current (Note 5)	$V_{HO} = 0 \text{ V}$ , $V_{IN} = 5 \text{ V}$ , $PW \leq 10 \mu\text{s}$	2.5	4.0	–	A
$I_{O-}$	Output Low, Short-Circuit Pulsed Current (Note 5)	$V_{HO} = 15 \text{ V}$ , $V_{IN} = 0 \text{ V}$ , $PW \leq 10 \mu\text{s}$	2.5	4.0	–	A
$V_S$	Allowable Negative $V_S$ Pin Voltage for IN Signal Propagation to HO		–	–	11	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. These parameters guaranteed by design.

**DYNAMIC ELECTRICAL CHARACTERISTICS** ( $V_{BIAS}$  ( $V_{DD}$ ,  $V_{BS}$ ) = 15 V,  $V_S = \text{GND} = 0 \text{ V}$ ,  $C_L = 1000 \text{ pF}$ , and  $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ , unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{ON}$	Turn-On Propagation Delay	$V_S = 0 \text{ V}$	–	48	100	ns
$t_{OFF}$	Turn-Off Propagation Delay	$V_S = 0 \text{ V}$	–	46	95	ns
$t_R$	Turn-On Rise Time		–	11	18	ns
$t_F$	Turn-Off Fall Time		–	12	19	ns

TYPICAL PERFORMANCE CHARACTERISTICS

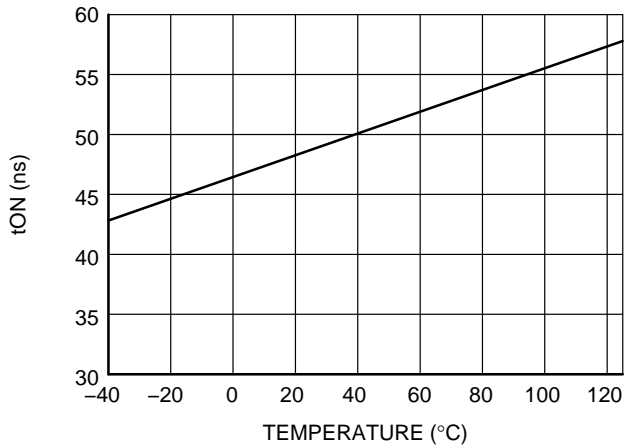


Figure 4. Turn-On Propagation Delay vs. Temperature

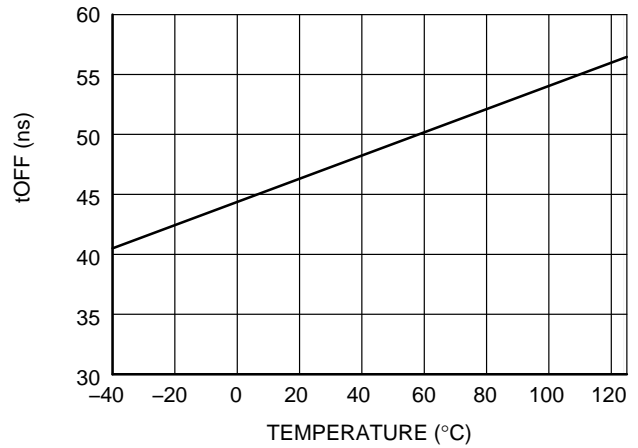


Figure 5. Turn-Off Propagation Delay vs. Temperature

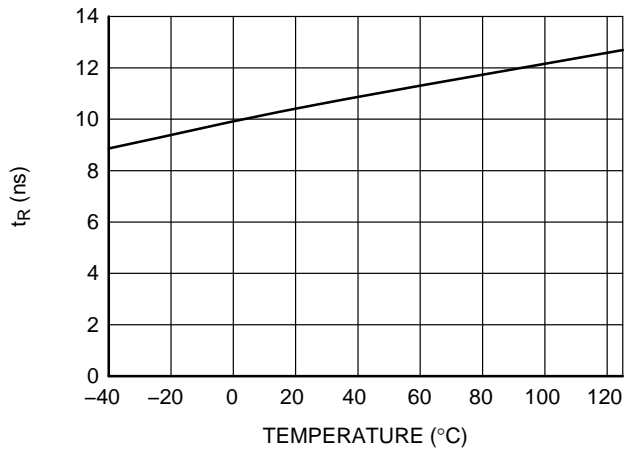


Figure 6. Turn-On Rise Time vs. Temperature

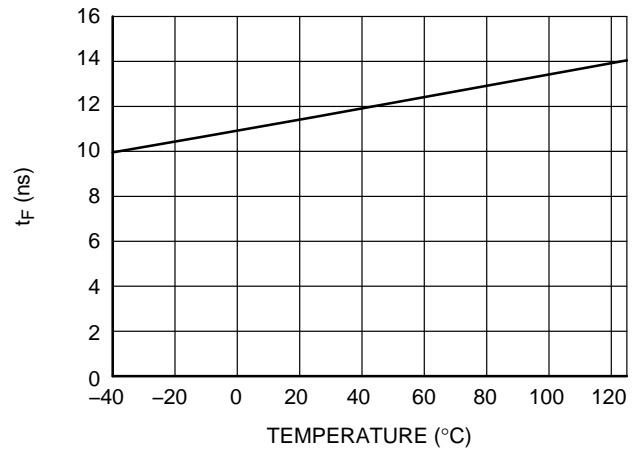


Figure 7. Turn-Off Fall Time vs. Temperature

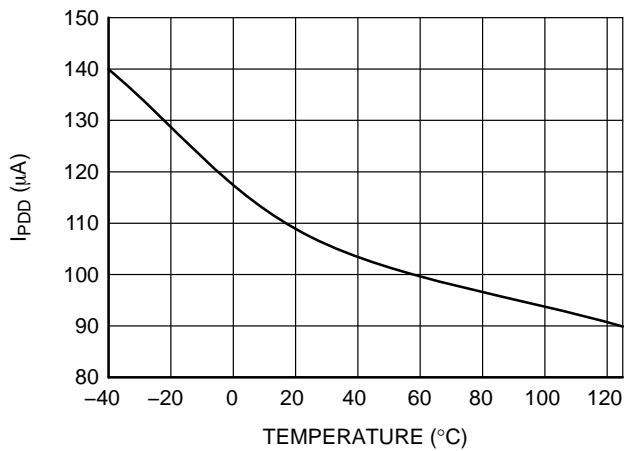


Figure 8. Operating V<sub>DD</sub> Supply Current vs. Temperature

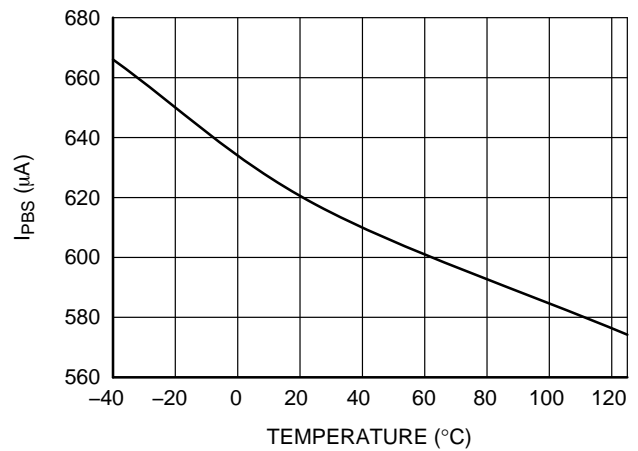


Figure 9. Operating V<sub>BS</sub> Supply Current vs. Temperature

# FAD7171MX

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

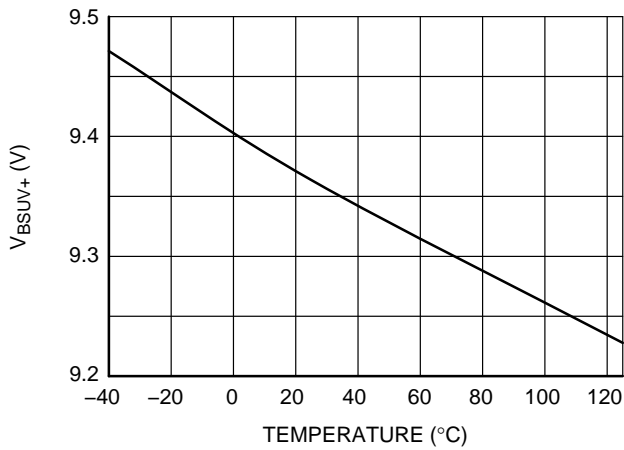


Figure 10.  $V_{BS}$  UVLO+ vs. Temperature

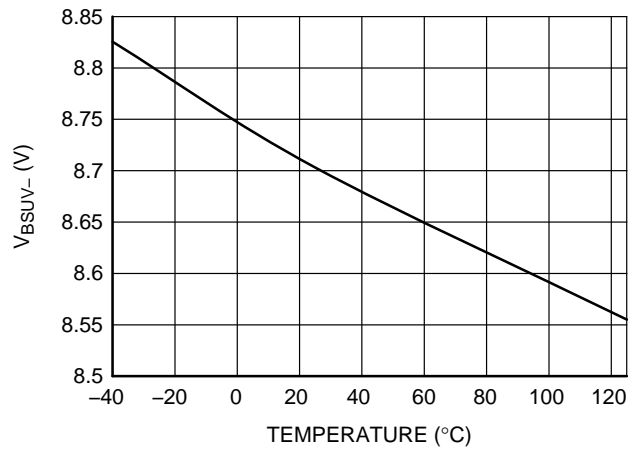


Figure 11.  $V_{BS}$  UVLO- vs. Temperature

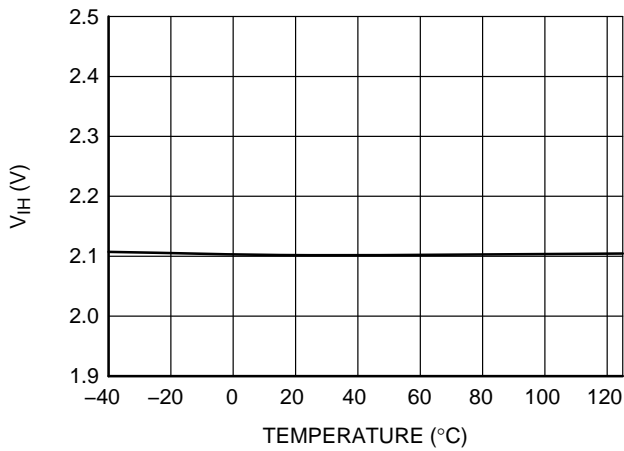


Figure 12. Logic High Input Voltage vs. Temperature

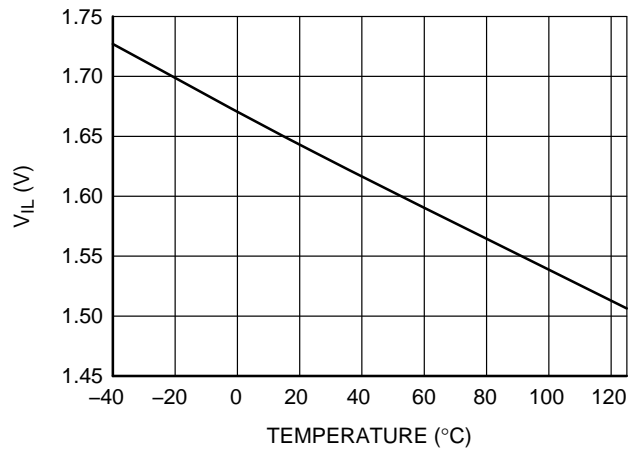


Figure 13. Logic Low Input Voltage vs. Temperature

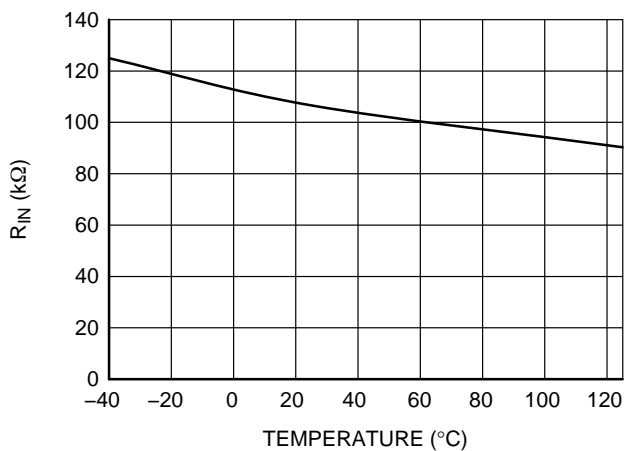


Figure 14.  $R_{IN}$  vs. Temperature

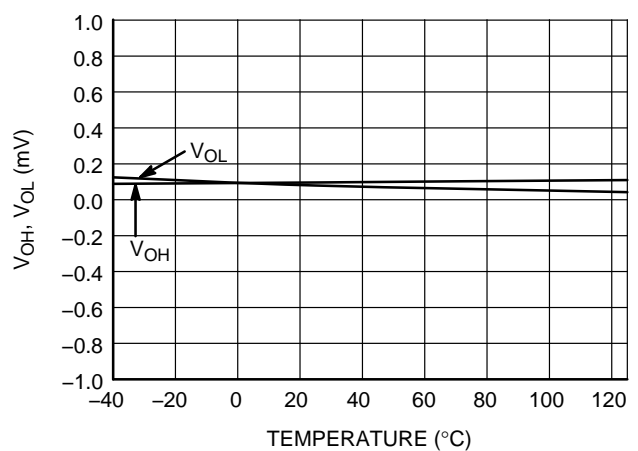


Figure 15. Output Voltage vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

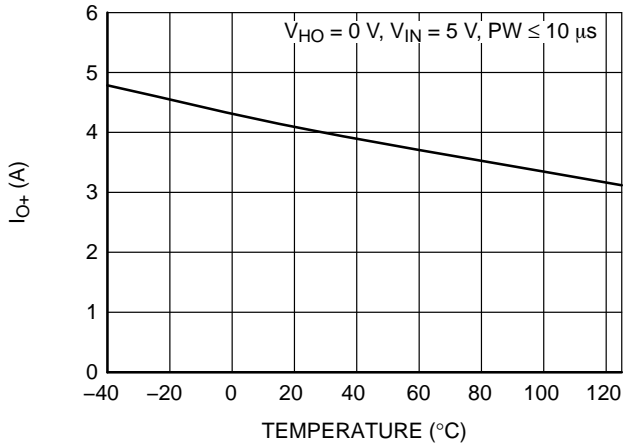


Figure 16. Output High, Short-Circuit Pulsed Current vs. Temperature

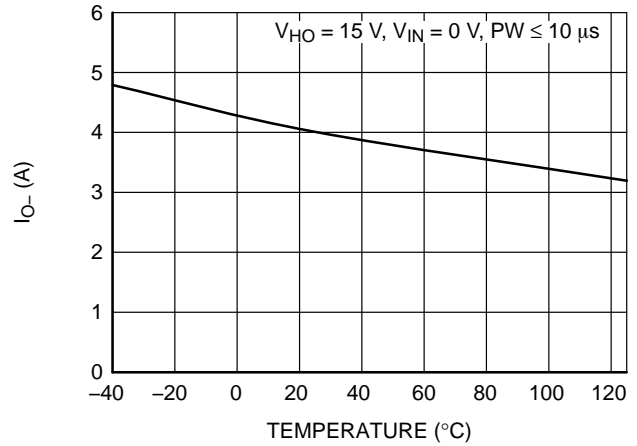


Figure 17. Output Low, Short-Circuit Pulsed Current vs. Temperature

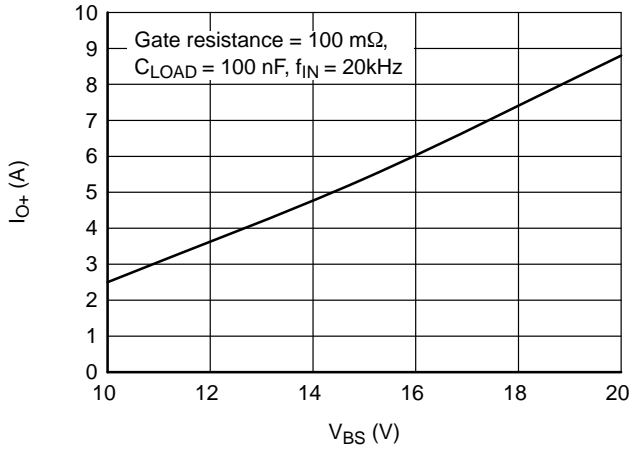


Figure 18. Output High, Short-Circuit Pulsed Current vs. Supply Voltage

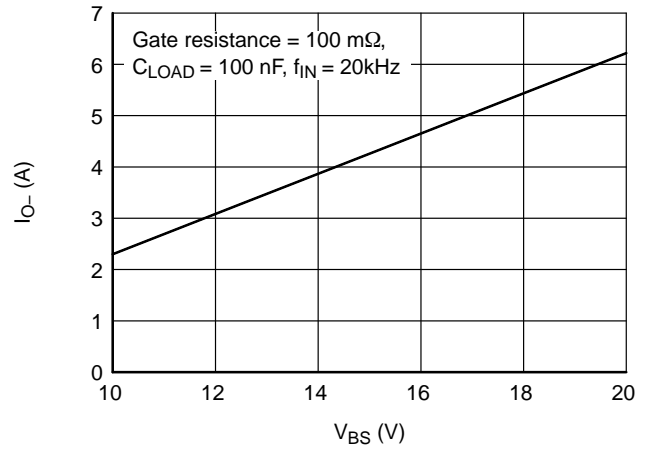


Figure 19. Output Low, Short-Circuit Pulsed Current vs. Supply Voltage

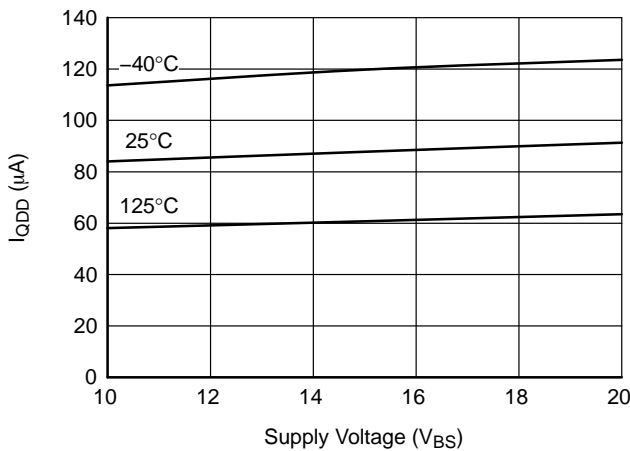


Figure 21. Quiescent  $V_{DD}$  Supply Current vs. Supply Voltage

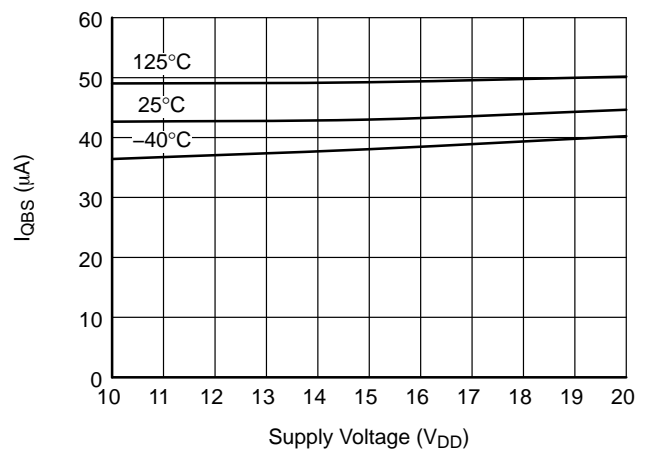


Figure 20. Quiescent  $V_{BS}$  Supply Current vs. Supply Voltage

# FAD7171MX

## SWITCHING TIME DEFINITIONS

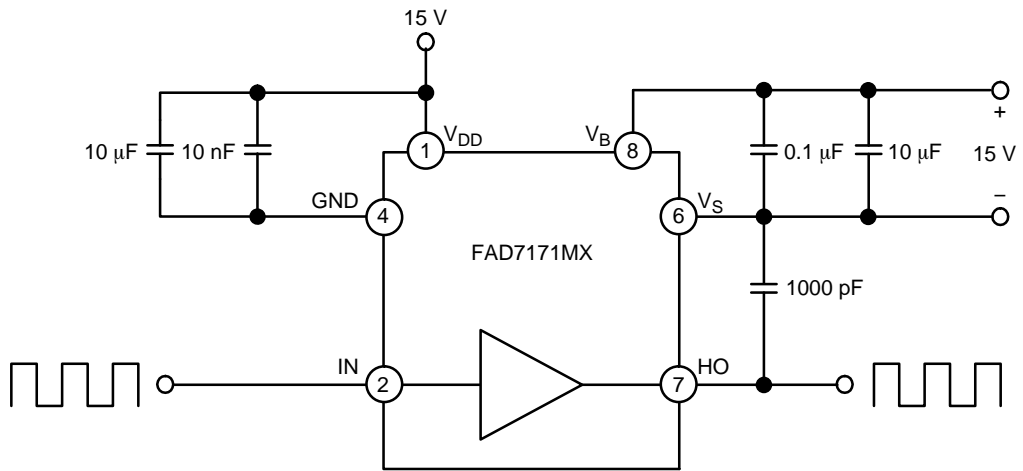


Figure 22. Switching Time Test Circuit (Referenced 8-SOIC)

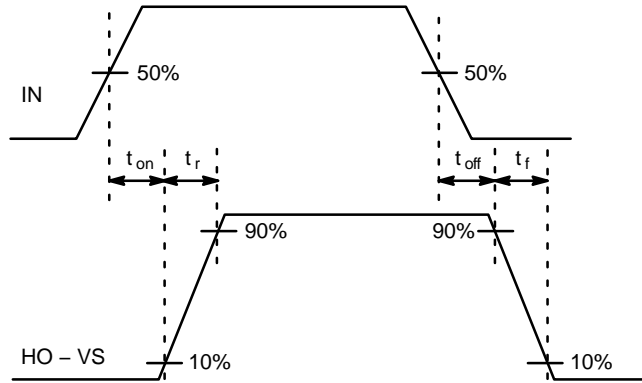
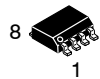


Figure 23. Switching Time Waveform Definitions





SCALE 1:1

SOIC-8 NB  
CASE 751-07  
ISSUE AK

DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-8 NB	PAGE 1 OF 2

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

- |   |  |  |  |
|---|--|--|--|
| <p>STYLE 1:<br/>         PIN 1. EMITTER<br/>         2. COLLECTOR<br/>         3. COLLECTOR<br/>         4. EMITTER<br/>         5. EMITTER<br/>         6. BASE<br/>         7. BASE<br/>         8. EMITTER</p>   | <p>STYLE 2:<br/>         PIN 1. COLLECTOR, DIE, #1<br/>         2. COLLECTOR, #1<br/>         3. COLLECTOR, #2<br/>         4. COLLECTOR, #2<br/>         5. BASE, #2<br/>         6. EMITTER, #2<br/>         7. BASE, #1<br/>         8. EMITTER, #1</p>               | <p>STYLE 3:<br/>         PIN 1. DRAIN, DIE #1<br/>         2. DRAIN, #1<br/>         3. DRAIN, #2<br/>         4. DRAIN, #2<br/>         5. GATE, #2<br/>         6. SOURCE, #2<br/>         7. GATE, #1<br/>         8. SOURCE, #1</p>                            | <p>STYLE 4:<br/>         PIN 1. ANODE<br/>         2. ANODE<br/>         3. ANODE<br/>         4. ANODE<br/>         5. ANODE<br/>         6. ANODE<br/>         7. ANODE<br/>         8. COMMON CATHODE</p>   |
| <p>STYLE 5:<br/>         PIN 1. DRAIN<br/>         2. DRAIN<br/>         3. DRAIN<br/>         4. DRAIN<br/>         5. GATE<br/>         6. GATE<br/>         7. SOURCE<br/>         8. SOURCE</p>   | <p>STYLE 6:<br/>         PIN 1. SOURCE<br/>         2. DRAIN<br/>         3. DRAIN<br/>         4. SOURCE<br/>         5. SOURCE<br/>         6. GATE<br/>         7. GATE<br/>         8. SOURCE</p>  | <p>STYLE 7:<br/>         PIN 1. INPUT<br/>         2. EXTERNAL BYPASS<br/>         3. THIRD STAGE SOURCE<br/>         4. GROUND<br/>         5. DRAIN<br/>         6. GATE 3<br/>         7. SECOND STAGE Vd<br/>         8. FIRST STAGE Vd</p>                    | <p>STYLE 8:<br/>         PIN 1. COLLECTOR, DIE #1<br/>         2. BASE, #1<br/>         3. BASE, #2<br/>         4. COLLECTOR, #2<br/>         5. COLLECTOR, #2<br/>         6. EMITTER, #2<br/>         7. EMITTER, #1<br/>         8. COLLECTOR, #1</p>                              |
| <p>STYLE 9:<br/>         PIN 1. EMITTER, COMMON<br/>         2. COLLECTOR, DIE #1<br/>         3. COLLECTOR, DIE #2<br/>         4. EMITTER, COMMON<br/>         5. EMITTER, COMMON<br/>         6. BASE, DIE #2<br/>         7. BASE, DIE #1<br/>         8. EMITTER, COMMON</p> | <p>STYLE 10:<br/>         PIN 1. GROUND<br/>         2. BIAS 1<br/>         3. OUTPUT<br/>         4. GROUND<br/>         5. GROUND<br/>         6. BIAS 2<br/>         7. INPUT<br/>         8. GROUND</p>  | <p>STYLE 11:<br/>         PIN 1. SOURCE 1<br/>         2. GATE 1<br/>         3. SOURCE 2<br/>         4. GATE 2<br/>         5. DRAIN 2<br/>         6. DRAIN 2<br/>         7. DRAIN 1<br/>         8. DRAIN 1</p>   | <p>STYLE 12:<br/>         PIN 1. SOURCE<br/>         2. SOURCE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>   |
| <p>STYLE 13:<br/>         PIN 1. N.C.<br/>         2. SOURCE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>  | <p>STYLE 14:<br/>         PIN 1. N-SOURCE<br/>         2. N-GATE<br/>         3. P-SOURCE<br/>         4. P-GATE<br/>         5. P-DRAIN<br/>         6. P-DRAIN<br/>         7. N-DRAIN<br/>         8. N-DRAIN</p>   | <p>STYLE 15:<br/>         PIN 1. ANODE 1<br/>         2. ANODE 1<br/>         3. ANODE 1<br/>         4. ANODE 1<br/>         5. CATHODE, COMMON<br/>         6. CATHODE, COMMON<br/>         7. CATHODE, COMMON<br/>         8. CATHODE, COMMON</p>               | <p>STYLE 16:<br/>         PIN 1. EMITTER, DIE #1<br/>         2. BASE, DIE #1<br/>         3. EMITTER, DIE #2<br/>         4. BASE, DIE #2<br/>         5. COLLECTOR, DIE #2<br/>         6. COLLECTOR, DIE #2<br/>         7. COLLECTOR, DIE #1<br/>         8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17:<br/>         PIN 1. VCC<br/>         2. V2OUT<br/>         3. V1OUT<br/>         4. TXE<br/>         5. RXE<br/>         6. VEE<br/>         7. GND<br/>         8. ACC</p>  | <p>STYLE 18:<br/>         PIN 1. ANODE<br/>         2. ANODE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. CATHODE<br/>         8. CATHODE</p>   | <p>STYLE 19:<br/>         PIN 1. SOURCE 1<br/>         2. GATE 1<br/>         3. SOURCE 2<br/>         4. GATE 2<br/>         5. DRAIN 2<br/>         6. MIRROR 2<br/>         7. DRAIN 1<br/>         8. MIRROR 1</p>   | <p>STYLE 20:<br/>         PIN 1. SOURCE (N)<br/>         2. GATE (N)<br/>         3. SOURCE (P)<br/>         4. GATE (P)<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>   |
| <p>STYLE 21:<br/>         PIN 1. CATHODE 1<br/>         2. CATHODE 2<br/>         3. CATHODE 3<br/>         4. CATHODE 4<br/>         5. CATHODE 5<br/>         6. COMMON ANODE<br/>         7. COMMON ANODE<br/>         8. CATHODE 6</p>  | <p>STYLE 22:<br/>         PIN 1. I/O LINE 1<br/>         2. COMMON CATHODE/VCC<br/>         3. COMMON CATHODE/VCC<br/>         4. I/O LINE 3<br/>         5. COMMON ANODE/GND<br/>         6. I/O LINE 4<br/>         7. I/O LINE 5<br/>         8. COMMON ANODE/GND</p> | <p>STYLE 23:<br/>         PIN 1. LINE 1 IN<br/>         2. COMMON ANODE/GND<br/>         3. COMMON ANODE/GND<br/>         4. LINE 2 IN<br/>         5. LINE 2 OUT<br/>         6. COMMON ANODE/GND<br/>         7. COMMON ANODE/GND<br/>         8. LINE 1 OUT</p> | <p>STYLE 24:<br/>         PIN 1. BASE<br/>         2. EMITTER<br/>         3. COLLECTOR/ANODE<br/>         4. COLLECTOR/ANODE<br/>         5. CATHODE<br/>         6. CATHODE<br/>         7. COLLECTOR/ANODE<br/>         8. COLLECTOR/ANODE</p>                                      |
| <p>STYLE 25:<br/>         PIN 1. VIN<br/>         2. N/C<br/>         3. REXT<br/>         4. GND<br/>         5. IOUT<br/>         6. IOUT<br/>         7. IOUT<br/>         8. IOUT</p>   | <p>STYLE 26:<br/>         PIN 1. GND<br/>         2. dv/dt<br/>         3. ENABLE<br/>         4. ILIMIT<br/>         5. SOURCE<br/>         6. SOURCE<br/>         7. SOURCE<br/>         8. VCC</p>  | <p>STYLE 27:<br/>         PIN 1. ILIMIT<br/>         2. OVLO<br/>         3. UVLO<br/>         4. INPUT+<br/>         5. SOURCE<br/>         6. SOURCE<br/>         7. SOURCE<br/>         8. DRAIN</p>  | <p>STYLE 28:<br/>         PIN 1. SW_TO_GND<br/>         2. DASIC OFF<br/>         3. DASIC_SW_DET<br/>         4. GND<br/>         5. V_MON<br/>         6. VBULK<br/>         7. VBULK<br/>         8. VIN</p>  |
| <p>STYLE 29:<br/>         PIN 1. BASE, DIE #1<br/>         2. EMITTER, #1<br/>         3. BASE, #2<br/>         4. EMITTER, #2<br/>         5. COLLECTOR, #2<br/>         6. COLLECTOR, #2<br/>         7. COLLECTOR, #1<br/>         8. COLLECTOR, #1</p>                        | <p>STYLE 30:<br/>         PIN 1. DRAIN 1<br/>         2. DRAIN 1<br/>         3. GATE 2<br/>         4. SOURCE 2<br/>         5. SOURCE 1/DRAIN 2<br/>         6. SOURCE 1/DRAIN 2<br/>         7. SOURCE 1/DRAIN 2<br/>         8. GATE 1</p>                           |  |  |

<b>DOCUMENT NUMBER:</b>	<b>98ASB42564B</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>SOIC-8 NB</b>	<b>PAGE 2 OF 2</b>

**onsemi** and **ONSEMI** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at [www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)