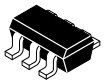
Single 2 A High-Speed, Low-Side Gate Driver

FAN3100T, FAN3100C

WDFN6 2x2, 065P
CASE 511CY



SOT23−5
CASE 527AH

Description

The FAN3100 2 A gate driver is designed to drive an N−channel enhancement−mode MOSFET in low−side switching applications by providing high peak current pulses during the short switching intervals. The driver is available with either TTL (FAN3100T) or CMOS (FAN3100C) input thresholds. Internal circuitry provides an under−voltage lockout function by holding the output LOW until the supply voltage is within the operating range. The FAN3100 delivers fast MOSFET switching performance, which helps maximize efficiency in high−frequency power converter designs.

FAN3100 drivers incorporate MillerDrive ™ architecture for the final output stage. This bipolar−MOSFET combination provides high peak current during the Miller plateau stage of the MOSFET turn−on / turn−off process to minimize switching loss, while providing rail−to−rail voltage swing and reverse current capability.

The FAN3100 also offers dual inputs that can be configured to operate in non−inverting or inverting mode and allow implementation of an enable function. If one or both inputs are left unconnected, internal resistors bias the inputs such that the output is pulled LOW to hold the power MOSFET off.

The FAN3100 is available in a lead−free finish, 2 × 2 mm, 6−lead, Molded Leadless Package (MLP) for the smallest size with excellent thermal performance; or industry−standard, 5−pin, SOT23.

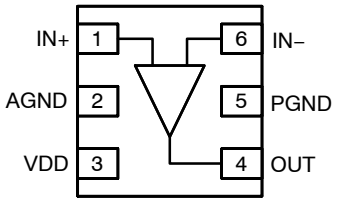
Features

- 3 A Peak Sink/Source at V_{DD} = 12 V
- 4.5 to 18 V Operating Range
- 2.5 A Sink/1.8 A Source at V_{OUT} = 6 V
- Dual−Logic Inputs Allow Configuration as Non−Inverting or Inverting with Enable Function
- Internal Resistors Turn Driver Off If No Inputs
- 13 ns Typical Rise Time and 9 ns Typical Fall−Time with 1 nF Load
- Choice of TTL or CMOS Input Thresholds
- MillerDrive Technology
- Typical Propagation Delay Time Under 20 ns with Input Falling or Rising
- 6−Lead, 2x2 mm MLP or 5−Pin, SOT23 Packages
- Rated from –40°C to 125°C Ambient
- These Devices are Pb−Free and Halogen Free

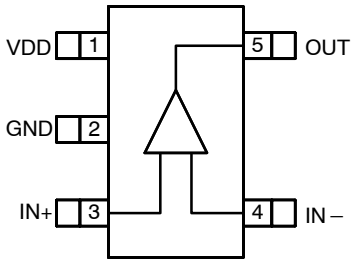
Applications

- Switch−Mode Power Supplies (SMPS)
- High−Efficiency MOSFET Switching
- Synchronous Rectifier Circuits
- DC−to−DC Converters
- Motor Control

PIN ASSIGNMENT

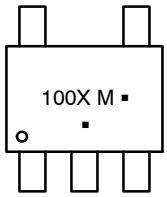


6−Lead MLP (Top View)



SOT23−5 (Top View)

MARKING DIAGRAM



100X = Specific Device Code
X = T or C
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 17 of this data sheet.

Block DiagramS

THERMAL CHARACTERISTICS (Note 1)

Package	Θ_{JL} (Note 2)	Θ_{JT} (Note 3)	Θ_{JA} (Note 4)	Ψ_{JB} (Note 5)	Ψ_{JT} (Note 6)	Unit
6−Lead, 2x2 mm Molded Leadless Package (MLP)	2.7	133	58	2.8	42	°C/W
SOT23, 5−Lead	56	99	157	51	5	°C/W

1. Estimates derived from thermal simulation; actual values depend on the application.
2. Theta_JL (Θ_{JL}): Thermal resistance between the semiconductor junction and the bottom surface of all the leads (including any thermal pad) that are typically soldered to a PCB.
3. Theta_JT (Θ_{JT}): Thermal resistance between the semiconductor junction and the top surface of the package, assuming it is held at a uniform temperature by a top−side heatsink.
4. Theta_JA (Θ_{JA}): Thermal resistance between junction and ambient, dependent on the PCB design, heat sinking, and airflow. The value given is for natural convection with no heatsink using a 2S2P board, as specified in JEDEC standards JESD51−2, JESD51−5, and JESD51−7, as appropriate.
5. Psi_JB (Ψ_{JB}): Thermal characterization parameter providing correlation between semiconductor junction temperature and an application circuit board reference point for the thermal environment defined in Note 4. For the MLP−6 package, the board reference is defined as the PCB copper connected to the thermal pad and protruding from either end of the package. For the SOT23−5 package, the board reference is defined as the PCB copper adjacent to pin 2.
6. Psi_JT (Ψ_{JT}): Thermal characterization parameter providing correlation between the semiconductor junction temperature and the center of the top of the package for the thermal environment defined in Note 4.

PIN DEFINITIONS

SOT23 Pin Number	MLP Pin Number	Name	Description
1	3	VDD	Supply Voltage. Provides power to the IC.
	2	AGND	Analog ground for input signals (MLP only). Connect to PGND underneath the IC.
2		GND	Ground (SOT−23 only). Common ground reference for input and output circuits.
3	1	IN+	Non−Inverting Input. Connect to VDD to enable output.
4	6	IN−	Inverting Input. Connect to AGND or PGND to enable output.
5	4	OUT	Gate Drive Output: Held LOW unless required inputs are present and V_{DD} is above UVLO threshold.
	Pad	P1	Thermal Pad (MLP only). Exposed metal on the bottom of the package, which is electrically connected to pin 5.
	5	PGND	Power Ground (MLP only). For output drive circuit; separates switching noise from inputs.

OUTPUT LOGIC

IN+	IN−	OUT
0 (Note 7)	0	0
0 (Note 7)	1 (Note 7)	0
1	0	1
1	1 (Note 7)	0

7. Default input signal if no external connection is made.

Block DiagramS

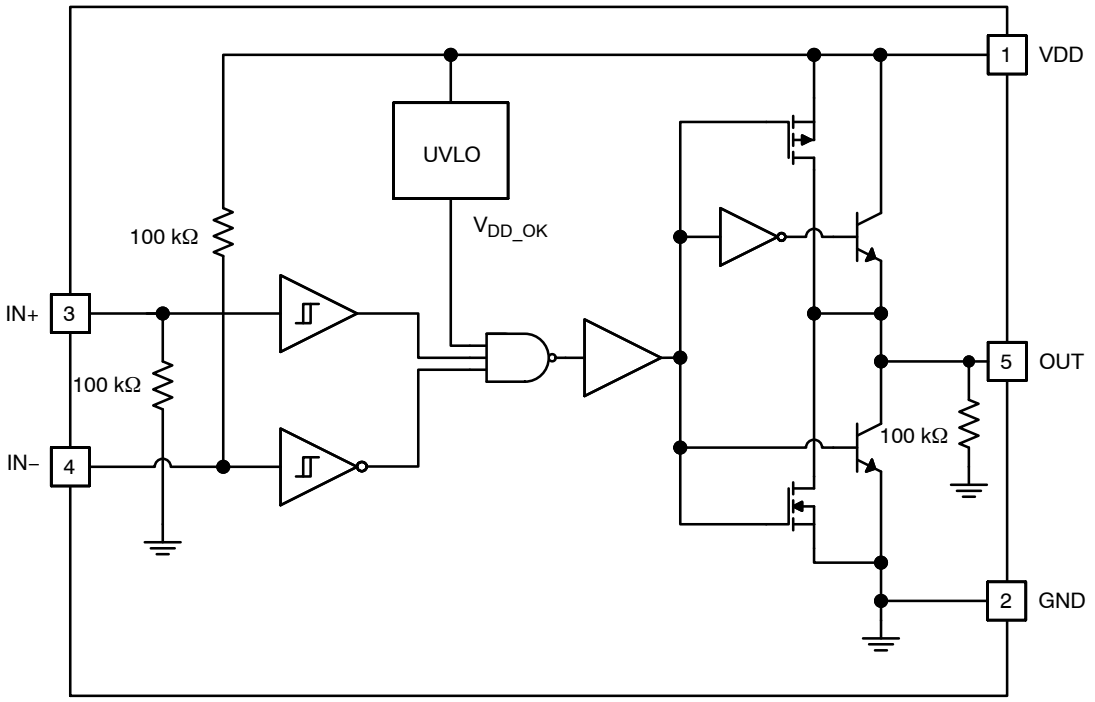


Figure 1. Simplified Block Diagram (SOT23 Pin−out)

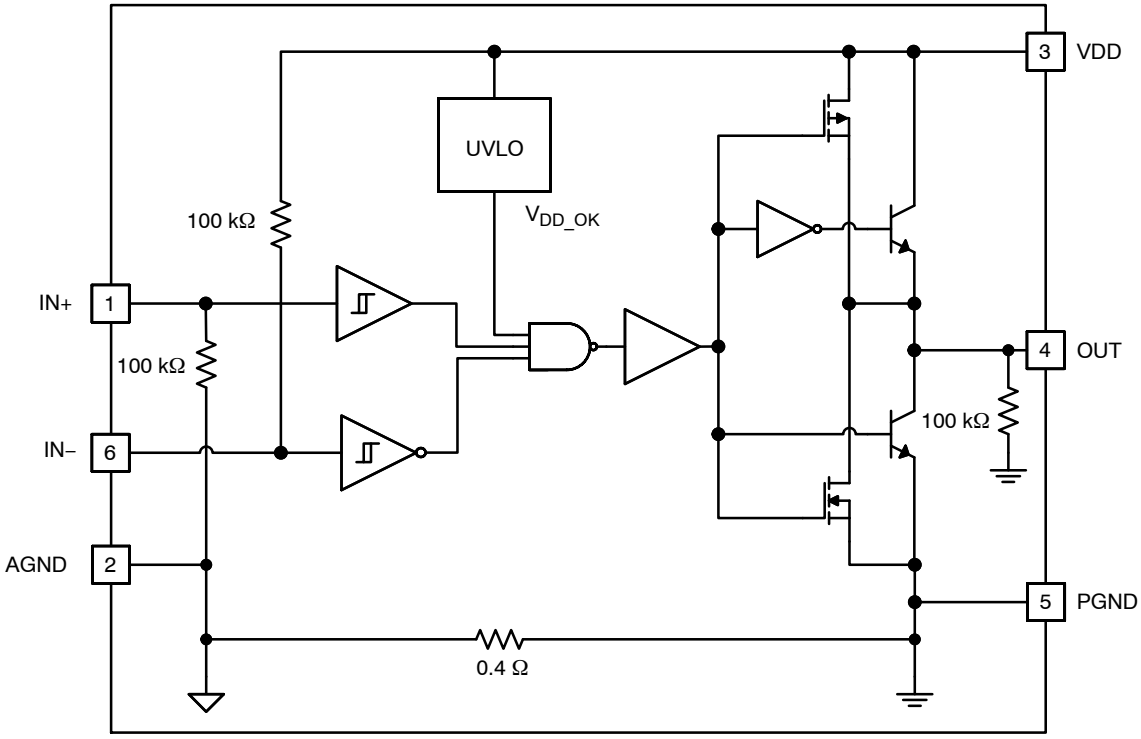


Figure 2. Simplified Block Diagram (MLP Pin−out)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
V_{DD}	VDD to GND	−0.3	20.0	V
V_{IN}	Voltage on IN+ and IN− to GND, AGND or PGND	GND −0.3	V_{DD} + 0.3	V
V_{OUT}	Voltage on OUT to GND, AGND or PGND	GND −0.3	V_{DD} + 0.3	V
	Repetitive Voltage on OUT to GND, AGND or PGND (T_{PULSE} < 300 ns) (Note 8)	GND −2	V_{DD} + 0.3	V
T_L	Lead Soldering Temperature (10 Seconds)		+260	°C
T_J	Junction Temperature	−55	+150	°C
T_{STG}	Storage Temperature	−65	+150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
8. Restricted by thermal dissipation. (< Max T_J)

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply Voltage Range	4.5	18.0	V
V_{IN}	Input Voltage IN+, IN−	0	V_{DD}	V
T_A	Operating Ambient Temperature	−40	+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (V_{DD} = 12 V, T_J = −40°C to +125°C unless otherwise noted. Currents are defined as positive into the device and negative out of the device.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
SUPPLY						
V_{DD}	Operating Range		4.5		18.0	V
I_{DD}	Supply Current Inputs/EN Not Connected	FAN3100C (Note 9)		0.20	0.35	mA
		FAN3100T		0.50	0.80	mA
V_{ON}	Turn−On Voltage		3.5	3.9	4.3	V
V_{OFF}	Turn−Off Voltage		3.3	3.7	4.1	V
INPUTS (FAN3100T)						
V_{INL_T}	IN+, IN− Logic Low−Voltage, Maximum		0.8			V
V_{INH_T}	IN+, IN− Logic High−Voltage, Minimum				2.0	V
I_{IN+}	Non−inverting Input	IN from 0 to V_{DD}	−1		175	μA
I_{IN-}	Inverting Input	IN from 0 to V_{DD}	−175		1	μA
V_{HYS}	IN+, IN− Logic Hysteresis Voltage		0.2	0.4	0.8	V
INPUTS (FAN3100C)						
V_{INL_C}	IN+, IN− Logic Low Voltage		30			%V_{DD}
V_{INH_C}	IN+, IN− Logic High Voltage				70	%V_{DD}
I_{INL}	IN Current, Low	IN from 0 to V_{DD}	−1		175	μA
I_{INH}	IN Current, High	IN from 0 to V_{DD}	−175		1	μA
V_{HYS_C}	IN+, IN− Logic Hysteresis Voltage			17		%V_{DD}
OUTPUT						
I_{SINK}	OUT Current, Mid−Voltage, Sinking (Note 10)	OUT at V_{DD}/2, C_{LOAD} = 0.1 μF, f = 1 kHz		2.5		A

ELECTRICAL CHARACTERISTICS (V_{DD} = 12 V, T_J = −40°C to +125°C unless otherwise noted. Currents are defined as positive into the device and negative out of the device.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OUTPUT						
I_{SOURCE}	OUT Current, Mid−Voltage, Sourcing (Note 10)	OUT at V_{DD}/2, C_{LOAD} = 0.1 μF, f = 1 kHz		−1.8		A
I_{PK_SINK}	OUT Current, Peak, Sinking (Note 10)	C_{LOAD} = 0.1 μF, f = 1kHz		3		A
I_{PK_SOURCE}	OUT Current, Peak, Sourcing (Note 10)	C_{LOAD} = 0.1 μF, f = 1 kHz		−3		A
t_{RISE}	Output Rise Time (Note 11)	C_{LOAD} = 1000 pF		13	20	ns
t_{FALL}	Output Fall Time (Note 11)	C_{LOAD} = 1000 pF		9	14	ns
t_{D1}, t_{D2}	Output Prop. Delay, CMOS Inputs (Note 11)	0−12 V_{IN}, 1 V/ns Slew Rate	7	15	28	ns
t_{D1}, t_{D2}	Output Prop. Delay, TTL Inputs (Note 11)	0−5 V_{IN}, 1 V/ns Slew Rate	9	16	30	ns
I_{RVS}	Output Reverse Current Withstand (Note 10)			500		mA

9. Lower supply current due to inactive TTL circuitry.
10. Not tested in production.
11. See Timing Diagrams of Figure 3 and Figure 4.

Timing Diagrams

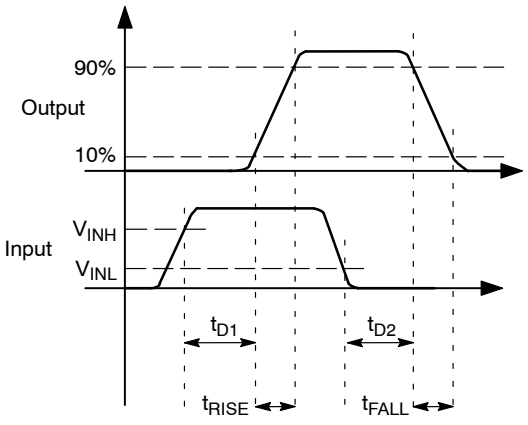


Figure 3. Non−Inverting

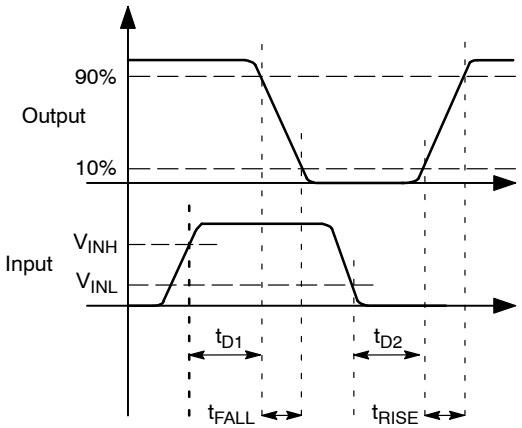


Figure 4. Inverting

Typical Performance Characteristics

(Typical characteristics are provided at 25°C and V_{DD} = 12 V unless otherwise noted)

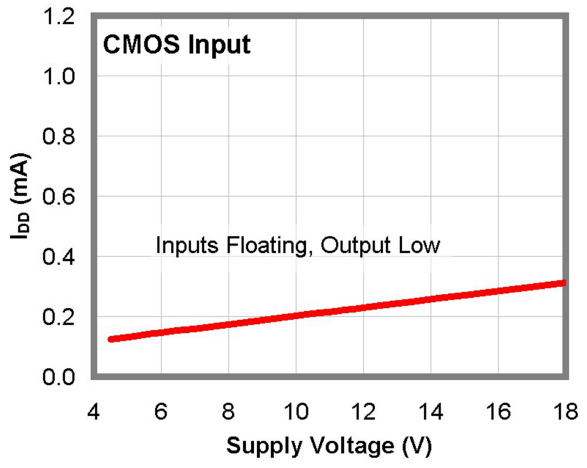


Figure 5. I_{DD} (Static) vs. Supply Voltage

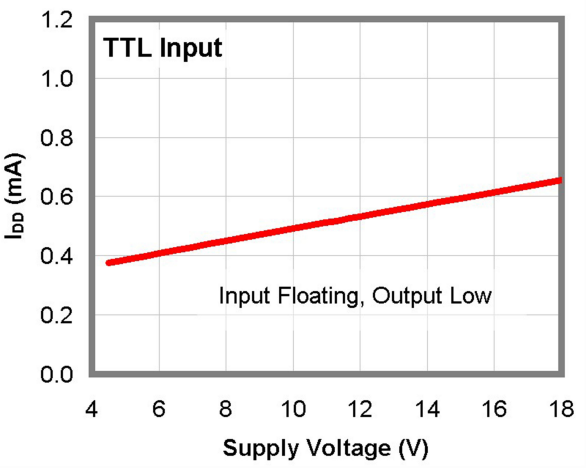


Figure 6. I_{DD} (Static) vs. Supply Voltage

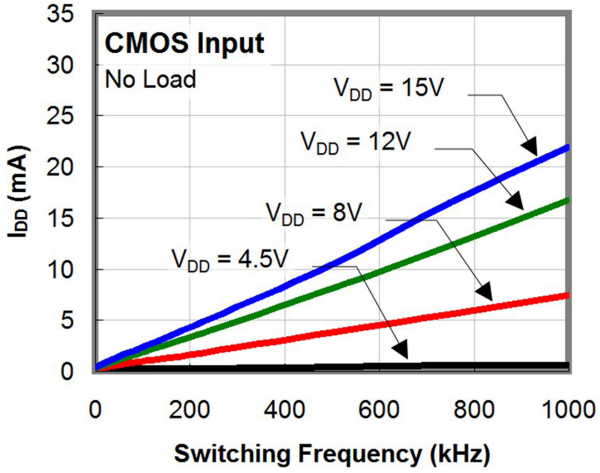


Figure 7. I_{DD} (No−Load) vs. Frequency

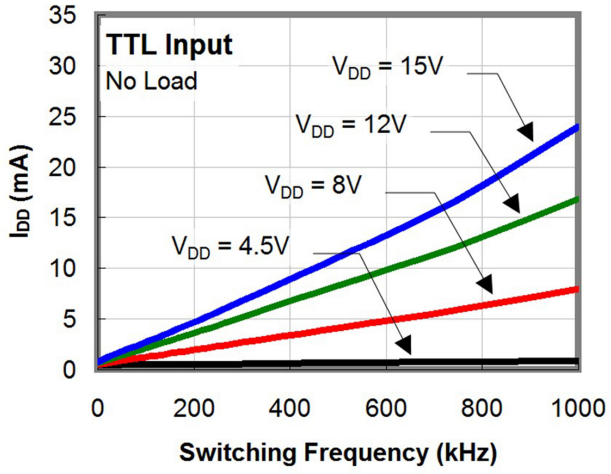


Figure 8. I_{DD} (No−Load) vs. Frequency

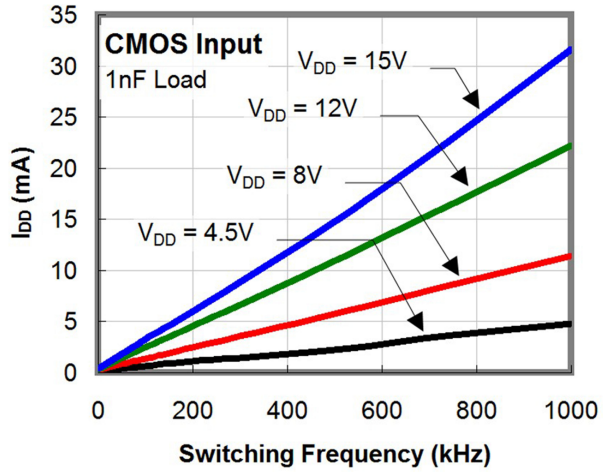


Figure 9. I_{DD} (1 nF Load) vs. Frequency

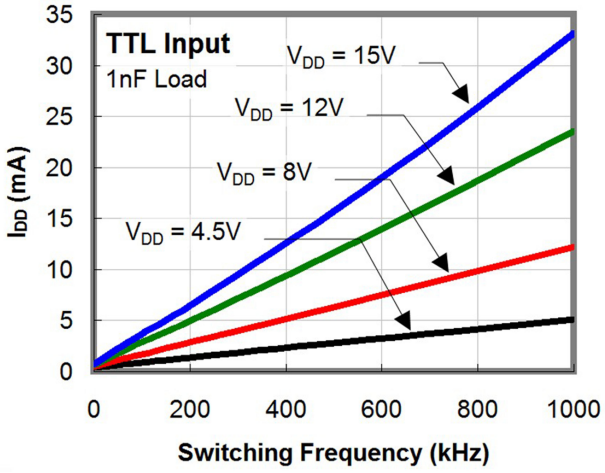


Figure 10. I_{DD} (1 nF Load) vs. Frequency

Typical Performance Characteristics (continued)

(Typical characteristics are provided at 25°C and V_{DD} = 12 V unless otherwise noted)

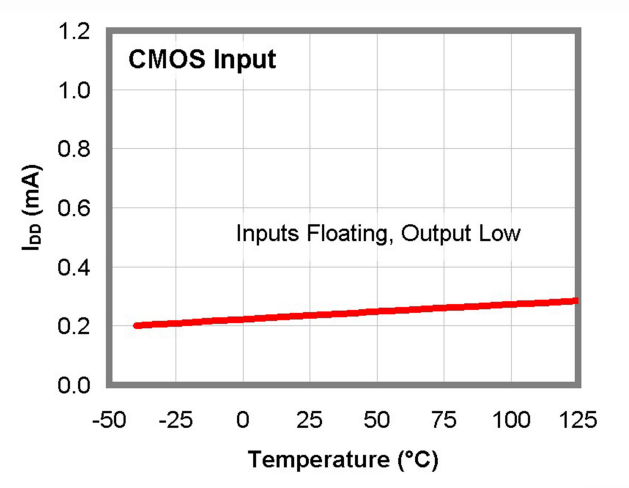


Figure 11. I_{DD} (Static) vs. Temperature

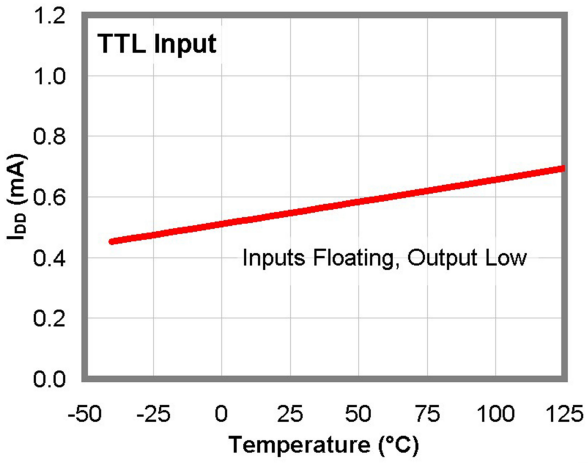


Figure 12. I_{DD} (Static) vs. Temperature

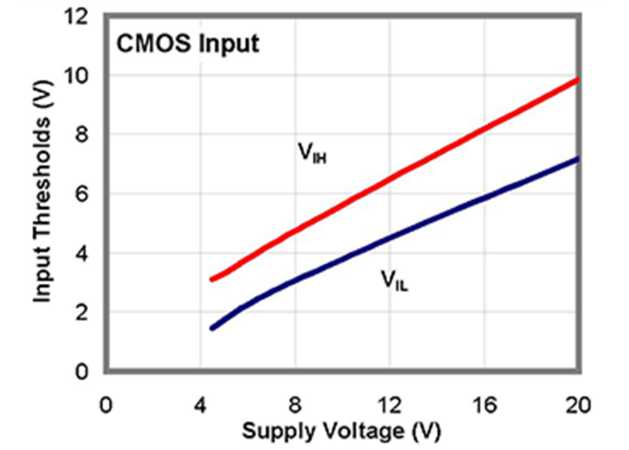


Figure 13. Input Thresholds vs. Supply Voltage

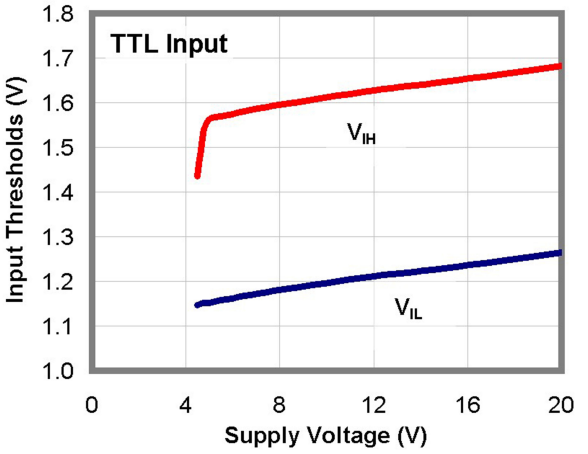


Figure 14. Input Thresholds vs. Supply Voltage

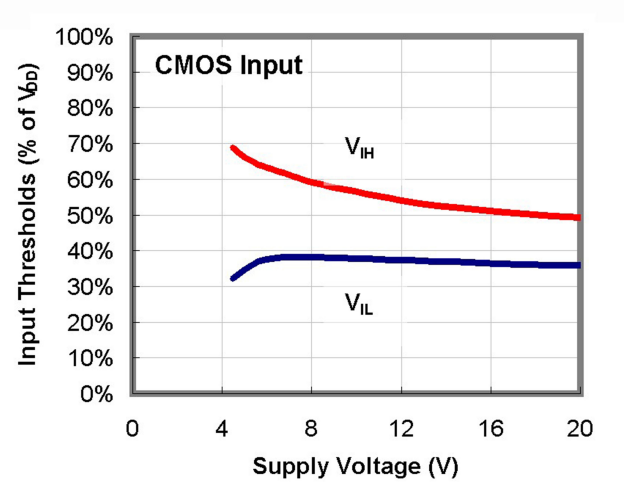


Figure 15. Input Thresholds % vs. Supply Voltage

Typical Performance Characteristics (continued)

(Typical characteristics are provided at 25°C and V_{DD} = 12 V unless otherwise noted)

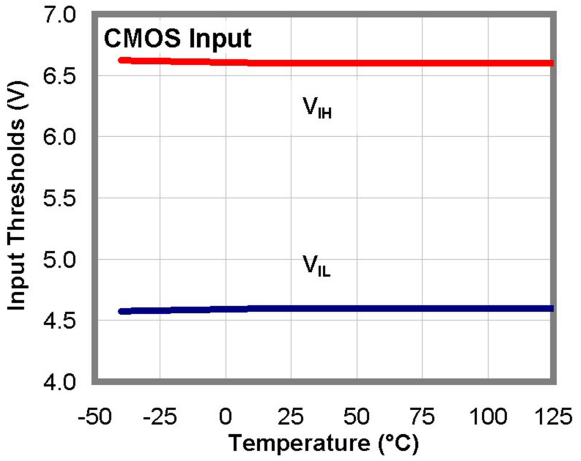


Figure 16. CMOS Input Thresholds vs. Temperature

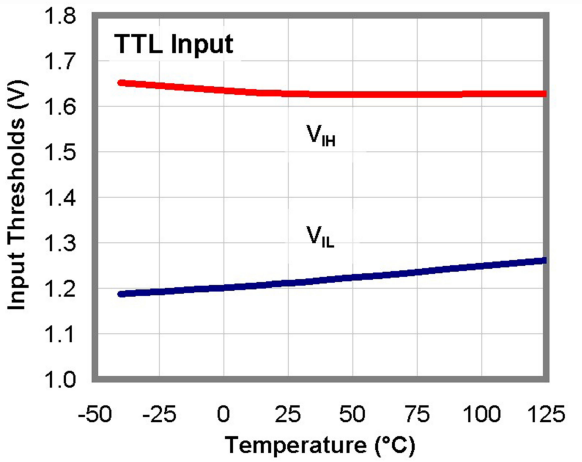


Figure 17. TTL Input Thresholds vs. Temperature

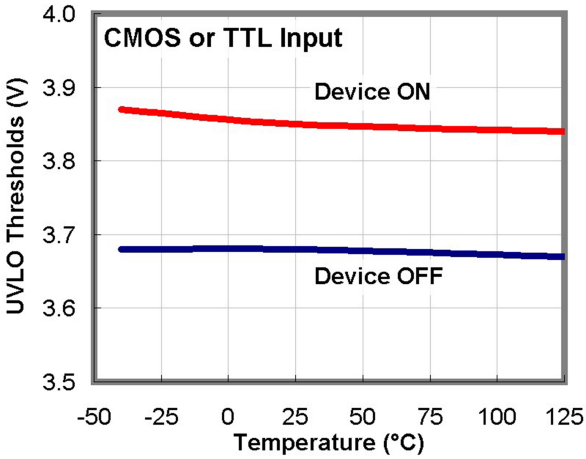


Figure 18. UVLO Thresholds vs. Temperature

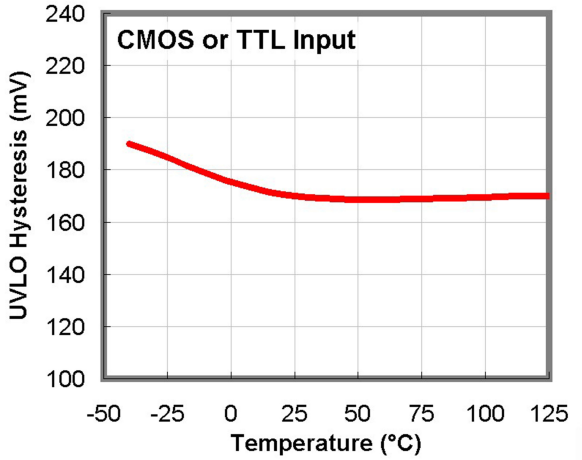


Figure 19. UVLO Hysteresis vs. Temperature

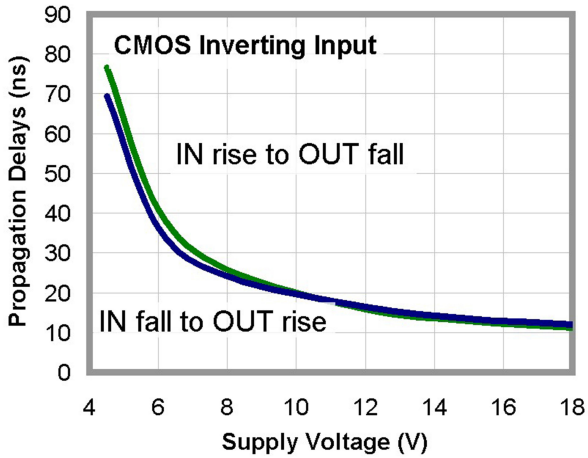


Figure 20. Propagation Delay vs. Supply Voltage

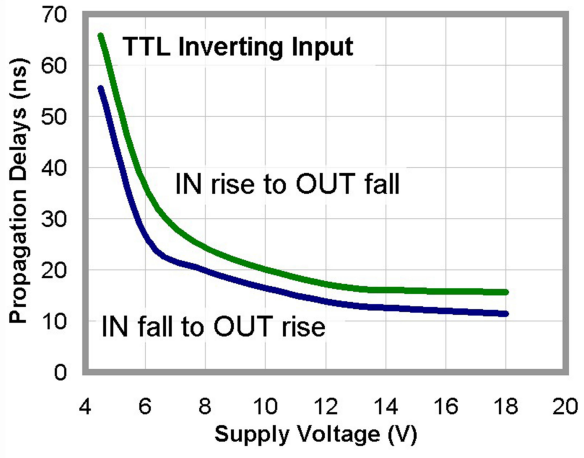


Figure 21. Propagation Delay vs. Supply Voltage

Typical Performance Characteristics (continued)

(Typical characteristics are provided at 25°C and V_{DD} = 12 V unless otherwise noted)

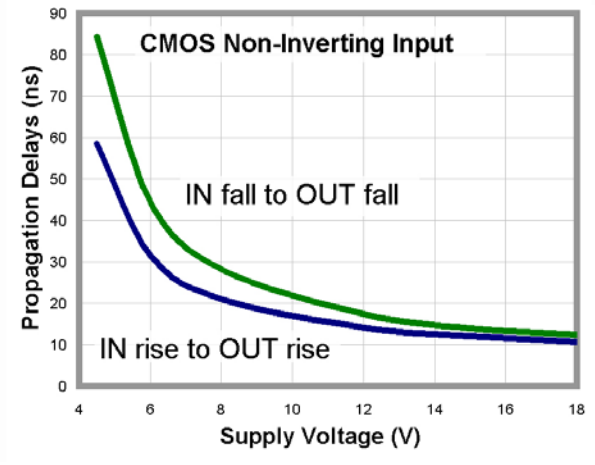


Figure 22. Propagation Delay vs. Supply Voltage

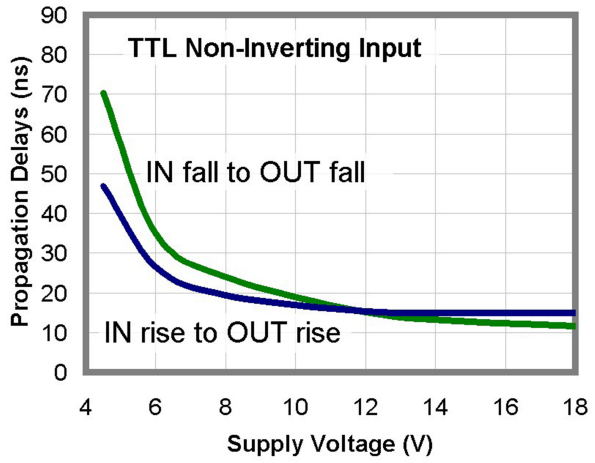


Figure 23. Propagation Delay vs. Supply Voltage

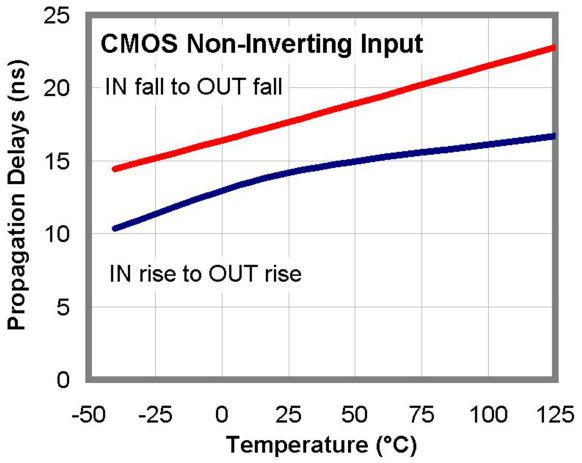


Figure 24. Propagation Delay vs. Temperature

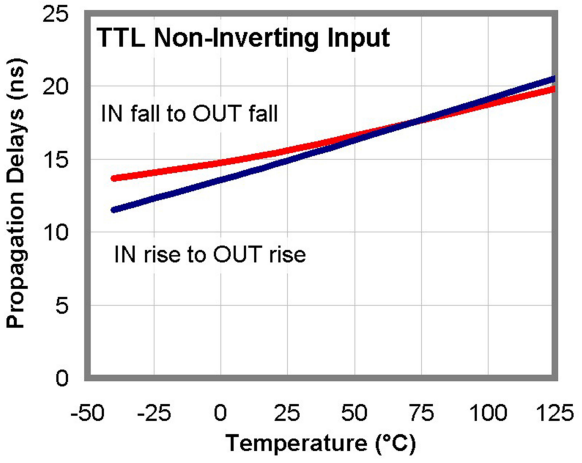


Figure 25. Propagation Delay vs. Temperature

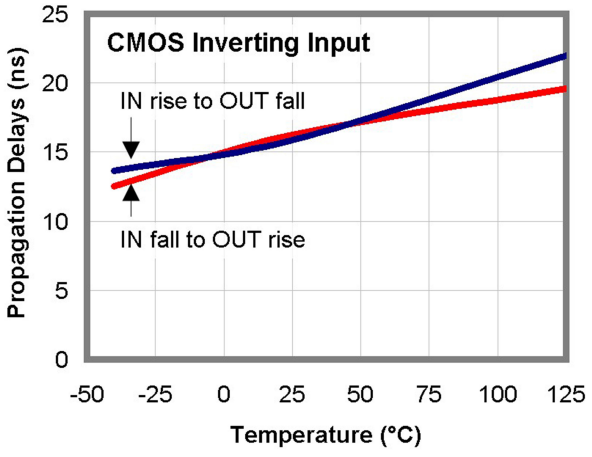


Figure 26. Propagation Delay vs. Temperature

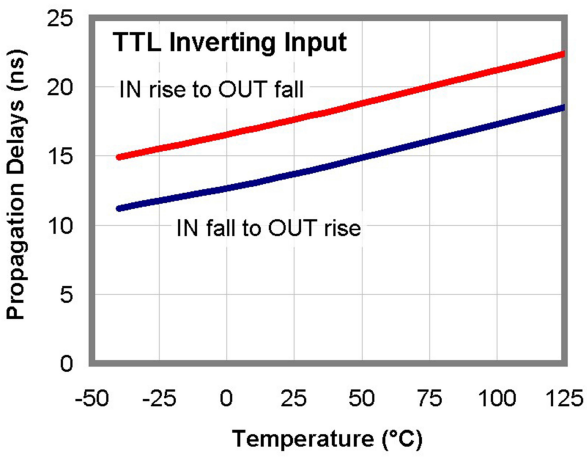


Figure 27. Propagation Delay vs. Temperature

Typical Performance Characteristics (continued)

(Typical characteristics are provided at 25°C and V_{DD} = 12 V unless otherwise noted)

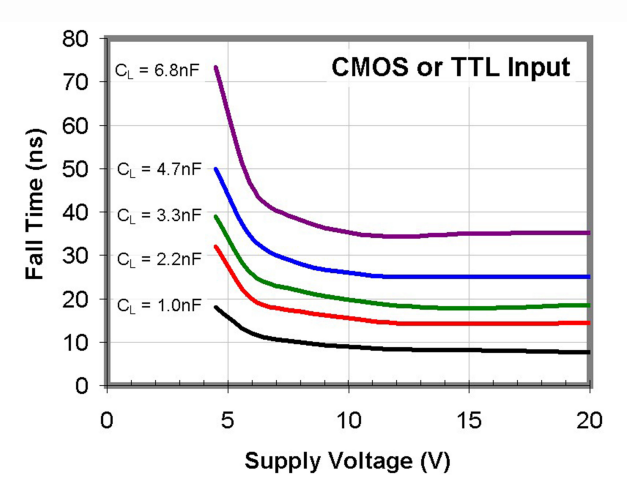


Figure 28. Fall Time vs. Supply Voltage

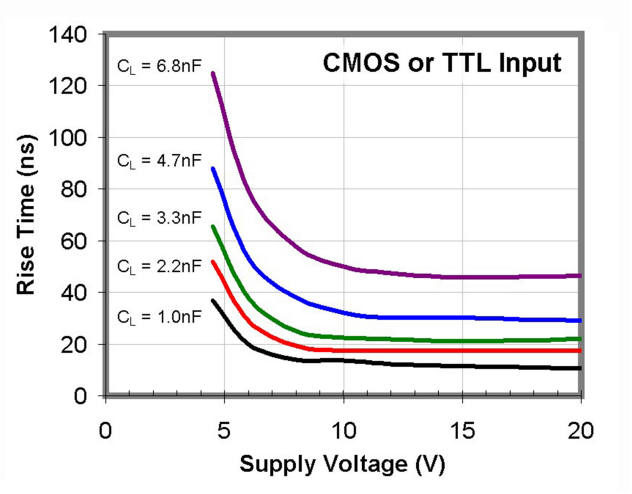


Figure 29. Rise Time vs. Supply Voltage

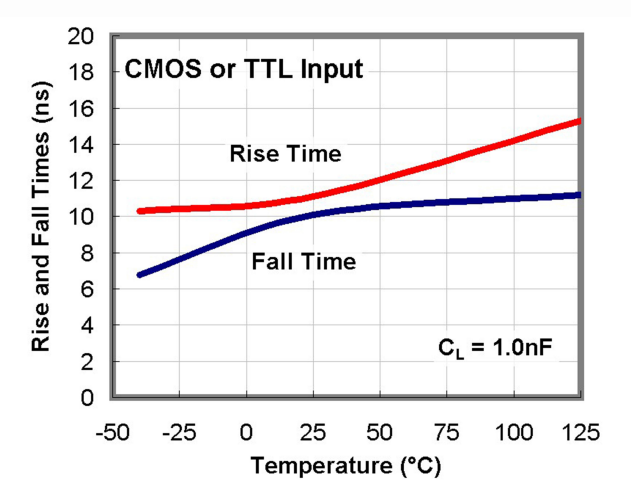


Figure 30. Rise and Fall Time vs. Temperature

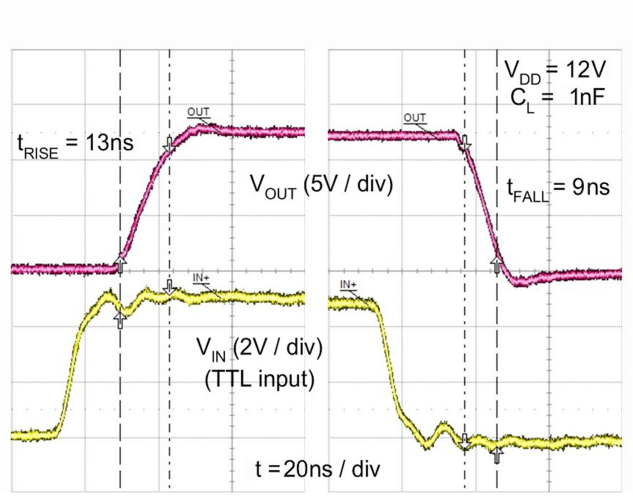


Figure 31. Rise / Fall Waveforms with 1 nF Load

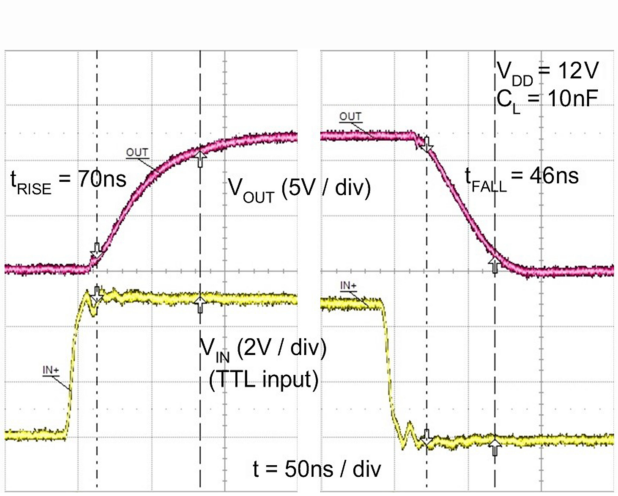


Figure 32. Rise / Fall Waveforms with 10 nF Load

Typical Performance Characteristics (continued)

(Typical characteristics are provided at 25°C and V_{DD} = 12 V unless otherwise noted)

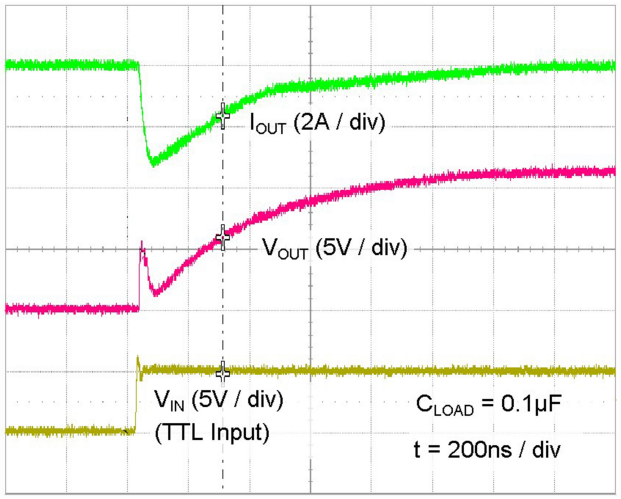


Figure 33. Quasi−Static Source Current with V_{DD} = 12 V

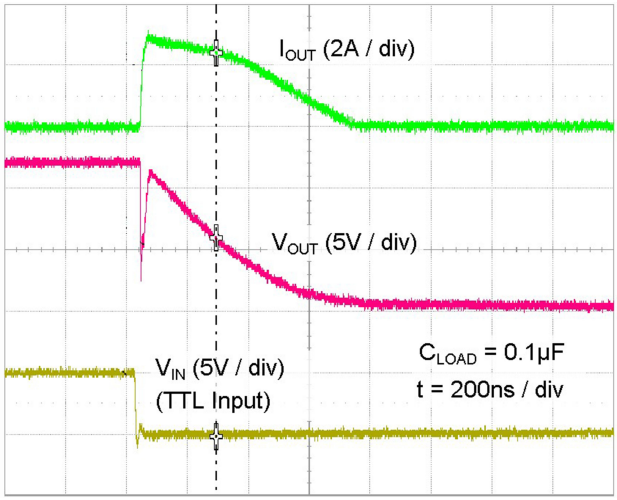


Figure 34. Quasi−Static Sink Current with V_{DD} = 12 V

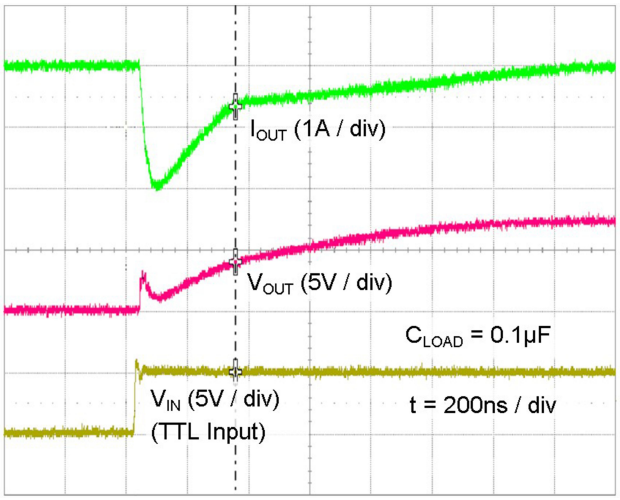


Figure 35. Quasi−Static Source Current with V_{DD} = 8 V

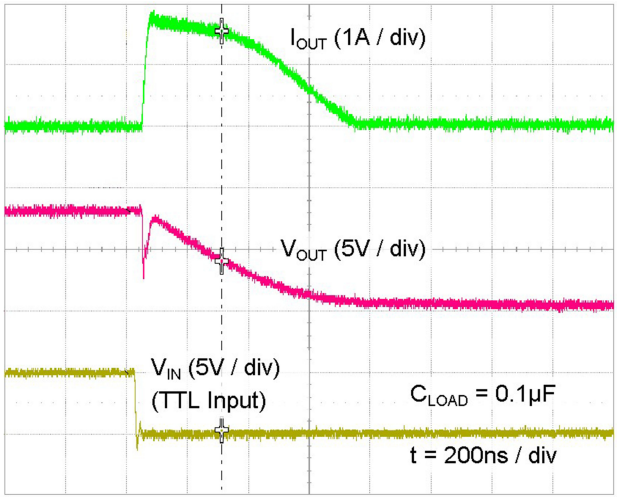


Figure 36. Quasi−Static Sink Current with V_{DD} = 8 V

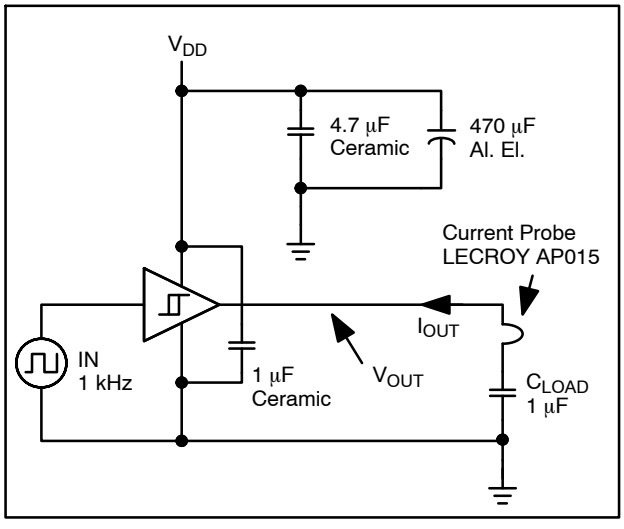


Figure 37. Quasi−Static I_{OUT} / V_{OUT} Test Circuit

Applications Information

Input Threshold

The FAN3100 offers TTL or CMOS input thresholds. In the FAN3100T, the input thresholds meet industry−standard TTL logic thresholds, independent of the V_{DD} voltage, and there is a hysteresis voltage of approximately 0.4 V. These levels permit the inputs to be driven from a range of input logic signal levels for which a voltage over 2 V is considered logic HIGH. The driving signal for the TTL inputs should have fast rising and falling edges with a slew rate of 6 V/μs or faster, so the rise time from 0 to 3.3 V should be 550 ns or less. With reduced slew rate, circuit noise could cause the driver input voltage to exceed the hysteresis voltage and retrigger the driver input, causing erratic operation. In the FAN3100C, the logic input thresholds are dependent on the V_{DD} level and, with V_{DD} of 12 V, the logic rising edge threshold is approximately 55% of V_{DD} and the input falling edge threshold is approximately 38% of V_{DD}. The CMOS input configuration offers a hysteresis voltage of approximately 17% of V_{DD}. The CMOS inputs can be used with relatively slow edges (approaching DC) if good decoupling and bypass techniques are incorporated in the system design to prevent noise from violating the input voltage hysteresis window. This allows setting precise timing intervals by fitting an R−C circuit between the controlling signal and the IN pin of the driver. The slow rising edge at the IN pin of the driver introduces a delay between the controlling signal and the OUT pin of the driver.

Static Supply Current

In the I_{DD} (static) typical performance graphs (Figure 5 – Figure 6 and Figure 11 – Figure 12), the curve is produced with all inputs floating (OUT is LOW) and indicates the lowest static I_{DD} current for the tested configuration. For other states, additional current flows through the 100 kΩ resistors on the inputs and outputs shown in the block diagrams (Figure 1 – Figure 2). In these cases, the actual static I_{DD} current is the value obtained from the curves plus this additional current.

MillerDrive™ Gate Drive Technology

FAN3100 drivers incorporate the MillerDrive architecture shown in Figure 38 for the output stage, a combination of bipolar and MOS devices capable of providing large currents over a wide range of supply voltage and temperature variations. The bipolar devices carry the bulk of the current as OUT swings between 1/3 to 2/3 V_{DD} and the MOS devices pull the output to the high or low rail.

The purpose of the MillerDrive architecture is to speed up switching by providing the highest current during the Miller plateau region when the gate−drain capacitance of the MOSFET is being charged or discharged as part of the turn−on / turn−off process. For applications that have zero voltage switching during the MOSFET turn−on or turn−off interval, the driver supplies high peak current for fast switching even though the Miller plateau is not present. This situation often occurs in synchronous rectifier applications because the body diode is generally conducting before the MOSFET is switched on. The output pin slew rate is determined by V_{DD} voltage and the load on the output. It is not user adjustable, but if a slower rise or fall time at the MOSFET gate is needed, a series resistor can be added.

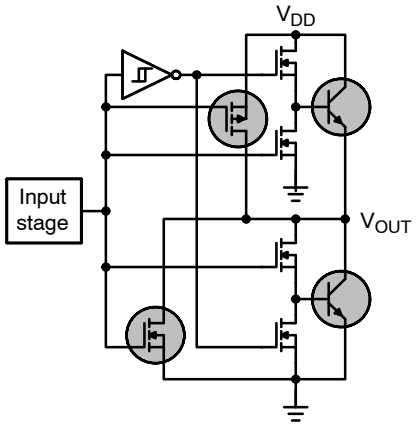


Figure 38. MillerDrive™ Output Architecture

Under−Voltage Lockout

The FAN3100 start−up logic is optimized to drive ground referenced N−channel MOSFETs with a under−voltage lockout (UVLO) function to ensure that the IC starts up in an orderly fashion. When V_{DD} is rising, yet below the 3.9 V operational level, this circuit holds the output LOW, regardless of the status of the input pins. After the part is active, the supply voltage must drop 0.2 V before the part shuts down. This hysteresis helps prevent chatter when low V_{DD} supply voltages have noise from the power switching. This configuration is not suitable for driving high−side P−channel MOSFETs because the low output voltage of the driver would turn the P−channel MOSFET on with V_{DD} below 3.9 V.

VDD Bypass Capacitor Guidelines

To enable this IC to turn a power device on quickly, a local, high−frequency, bypass capacitor C_{BYP} with low ESR and ESL should be connected between the VDD and GND pins with minimal trace length. This capacitor is in addition to bulk electrolytic capacitance of 10 μF to 47 μF often found on driver and controller bias circuits.

A typical criterion for choosing the value of C_{BYP} is to keep the ripple voltage on the V_{DD} supply ≤ 5%. Often this is achieved with a value ≥ 20 times the equivalent load capacitance C_{EQV}, defined here as Q_{gate}/V_{DD}. Ceramic capacitors of 0.1 μF to 1 μF or larger are common choices, as are dielectrics, such as X5R and X7R, which have good temperature characteristics and high pulse current capability.

If circuit noise affects normal operation, the value of C_{BYP} may be increased to 50−100 times the C_{EQV}, or C_{BYP} may be split into two capacitors. One should be a larger value, based on equivalent load capacitance, and the other a smaller value, such as 1−10 nF, mounted closest to the VDD and GND pins to carry the higher−frequency components of the current pulses.

Layout and Connection Guidelines

The FAN3100 incorporates fast−reacting input circuits, short propagation delays, and powerful output stages capable of delivering current peaks over 2 A to facilitate voltage transition times from under 10 ns to over 100 ns. The following layout and connection guidelines are strongly recommended:

- Keep high−current output and power ground paths separate from logic input signals and signal ground paths. This is especially critical when dealing with TTL−level logic thresholds.
- Keep the driver as close to the load as possible to minimize the length of high−current traces. This reduces the series inductance to improve high−speed switching, while reducing the loop area that can radiate EMI to the driver inputs and other surrounding circuitry.
- The FAN3100 is available in two packages with slightly different pinouts, offering similar performance. In the 6−pin MLP package, Pin 2 is internally connected to the input analog ground and should be connected to power ground, Pin 5, through a short direct path underneath the IC. In the 5−pin SOT23, the internal analog and power ground connections are made through separate, individual bond wires to Pin 2, which should be used as the common ground point for power and control signals.
- Many high−speed power circuits can be susceptible to noise injected from their own output or other external sources, possibly causing output re−triggering. These effects can be especially obvious if the circuit is tested in breadboard or non−optimal circuit layouts with long input, enable, or output leads. For best results, make connections to all pins as short and direct as possible.
- The turn−on and turn−off current paths should be minimized as discussed in the following sections.

Figure 39 shows the pulsed gate drive current path when the gate driver is supplying gate charge to turn the MOSFET on. The current is supplied from the local bypass capacitor, C_{BYP}, and flows through the driver to the MOSFET gate and to ground. To reach the high peak currents possible, the resistance and inductance in the path should be minimized. The localized C_{BYP} acts to contain the high peak current pulses within this driver−MOSFET circuit, preventing them from disturbing the sensitive analog circuitry in the PWM controller.

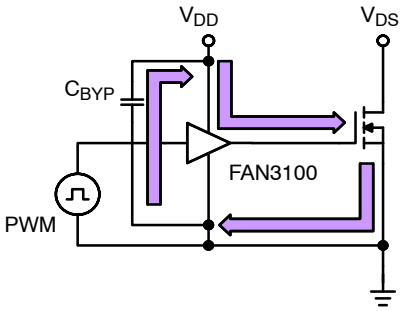


Figure 39. Current Path for MOSFET Turn−On

Figure 40 shows the current path when the gate driver turns the MOSFET off. Ideally, the driver shunts the current directly to the source of the MOSFET in a small circuit loop. For fast turn−off times, the resistance and inductance in this path should be minimized.

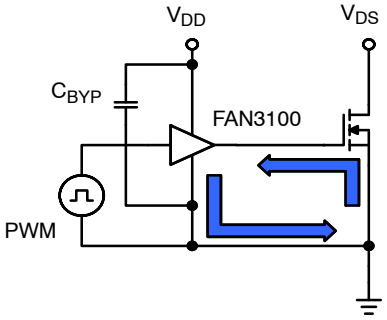


Figure 40. Current Path for MOSFET Turn−Off

Truth Table of Logic Operation

The truth table indicates the operational states using the dual−input configuration. In a non−inverting driver configuration, the IN− pin should be a logic LOW signal. If the IN− pin is connected to logic HIGH, a disable function is realized, and the driver output remains LOW regardless of the state of the IN+ pin.

Table 1. FAN3100 TRUTH TABLE

IN+	IN−	OUT
0	0	0
0	1	0
1	0	1
1	1	0

In the non−inverting driver configuration in Figure 41, the IN− pin is tied to ground and the input signal (PWM) is applied to IN+ pin. The IN− pin can be connected to logic HIGH to disable the driver and the output remains LOW,

regardless of the state of the IN+ pin.

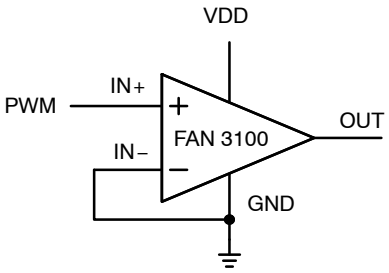


Figure 41. Dual−Input Driver Enabled, Non−Inverting Configuration

In the inverting driver application shown in Figure 42, the IN+ pin is tied HIGH. Pulling the IN+ pin to GND forces the output LOW, regardless of the state of the IN− pin.

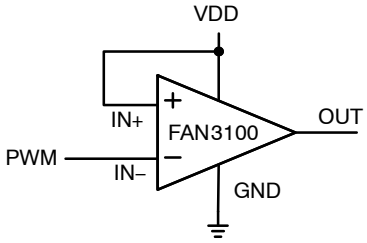


Figure 42. Dual−Input Driver Enabled, Inverting Configuration

Operational Waveforms

At power up, the driver output remains LOW until the V_{DD} voltage reaches the turn−on threshold. The magnitude of the OUT pulses rises with V_{DD} until steady−state V_{DD} is reached. The non−inverting operation illustrated in Figure 43 shows that the output remains LOW until the UVLO threshold is reached, then the output is in−phase with the input.

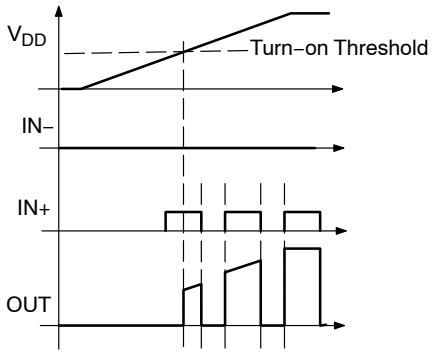


Figure 43. Non−Inverting Start−Up Waveforms

For the inverting configuration of Figure 42, start−up waveforms are shown in Figure 44. With IN+ tied to VDD and the input signal applied to IN−, the OUT pulses are inverted with respect to the input. At power up, the inverted output remains LOW until the V_{DD} voltage reaches the turn−on threshold, then it follows the input with inverted phase.

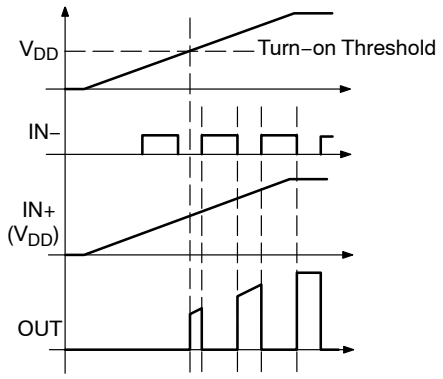


Figure 44. Inverting Start−Up Waveforms

Thermal Guidelines

Gate drivers used to switch MOSFETs and IGBTs at high frequencies can dissipate significant amounts of power. It is important to determine the driver power dissipation and the resulting junction temperature in the application to ensure that the part is operating within acceptable temperature limits.

The total power dissipation in a gate driver is the sum of two components; P_{GATE} and $P_{DYNAMIC}$:

$$P_{TOTAL} = P_{GATE} + P_{DYNAMIC} \quad \text{(eq. 1)}$$

Gate Driving Loss: The most significant power loss results from supplying gate current (charge per unit time) to switch the load MOSFET on and off at the switching frequency. The power dissipation that results from driving a MOSFET at a specified gate−source voltage, V_{GS}, with gate charge, Q_G, at switching frequency, f_{SW}, is determined by:

$$P_{GATE} = Q_G \cdot V_{GS} \cdot f_{SW} \quad \text{(eq. 2)}$$

Dynamic Pre−drive / Shoot−through Current: A power loss resulting from internal current consumption under dynamic operating conditions, including pin pull−up / pull−down resistors, can be obtained using the *I_{DD} (no−Load) vs. Frequency* graphs in Typical Performance Characteristics to determine the current $I_{DYNAMIC}$ drawn from V_{DD} under actual operating conditions:

$$P_{DYNAMIC} = I_{DYNAMIC} \cdot V_{DD} \quad \text{(eq. 3)}$$

Once the power dissipated in the driver is determined, the driver junction rise with respect to circuit board can be evaluated using the following thermal equation, assuming Ψ_{JB} was determined for a similar thermal design (heat sinking and air flow):

$$T_J = P_{TOTAL} \cdot \Psi_{JB} + T_B \quad \text{(eq. 4)}$$

where:

T_J = driver junction temperature;

Ψ_{JB} = (psi) thermal;
characterization parameter relating temperature rise to total power dissipation;

T_B = board temperature in location defined in the Thermal Characteristics table

In a typical forward converter application with 48 V input, as shown in Figure 45, the FDS2672 would be a potential MOSFET selection. The typical gate charge would be 32 nC with $V_{GS} = V_{DD} = 10$ V. Using a TTL input driver at a switching frequency of 500 kHz, the total power dissipation can be calculated as:

$$P_{GATE} = 32nC \cdot 10V \cdot 500kHz = 0.160W \quad \text{(eq. 5)}$$

$$P_{DYNAMIC} = 8mA \cdot 10V = 0.080W \quad \text{(eq. 6)}$$

$$P_{TOTAL} = 0.24W \quad \text{(eq. 7)}$$

The 5−pin SOT23 has a junction−to−lead thermal characterization parameter $\Psi_{JB} = 51°C/W$.

In a system application, the localized temperature around the device is a function of the layout and construction of the PCB along with airflow across the surfaces. To ensure reliable operation, the maximum junction temperature of the device must be prevented from exceeding the maximum rating of 150°C; with 80% derating, T_J would be limited to 120°C. Rearranging Equation 4 determines the board temperature required to maintain the junction temperature below 120°C:

$$T_{B,MAX} = T_J - P_{TOTAL} \cdot \Psi_{JB} \quad \text{(eq. 8)}$$

$$T_{B,MAX} = 120°C - 0.24W \cdot 51°C/W = 108°C \quad \text{(eq. 9)}$$

For comparison purposes, replace the 5−pin SOT23 used in the previous example with the 6−pin MLP package with $\Psi_{JB} = 2.8°C/W$. The 6−pin MLP package can operate at a PCB temperature of 119°C, while maintaining the junction temperature below 120°C. This illustrates that the physically smaller MLP package with thermal pad offers a more conductive path to remove the heat from the driver. Consider the tradeoffs between reducing overall circuit size with junction temperature reduction for increased reliability.

TYPICAL Application DIAGRAMS

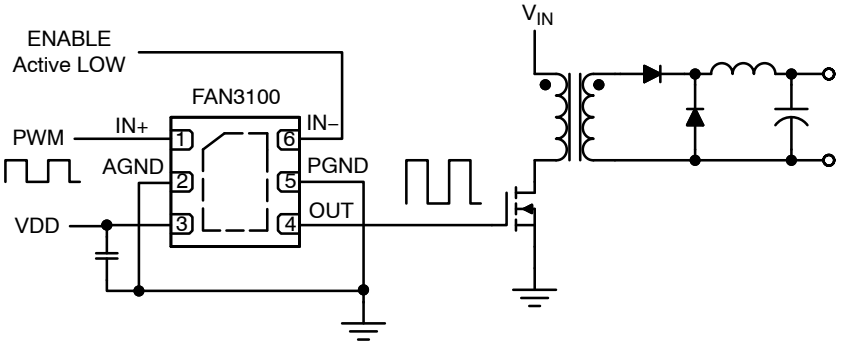


Figure 45. Forward Converter, Primary−Side Gate Drive (MLP Package Show)

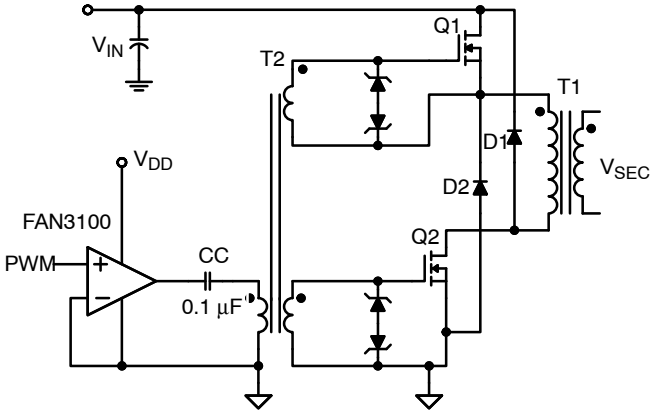


Figure 46. Driver for Two−Transistor Forward Converter Gate Transformer

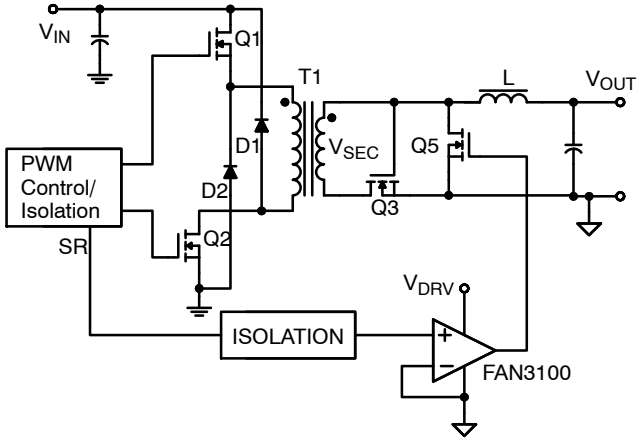


Figure 47. Secondary Synchronous Rectifier Driver

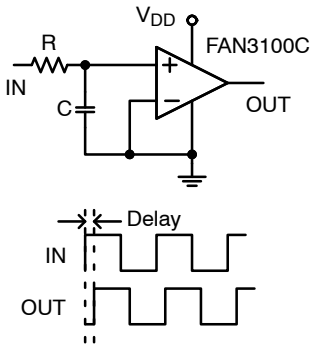


Figure 48. Programmable Delay Using CMOS Input

ORDERING INFORMATION

Part Number	Input Threshold	Package	Shipping†
FAN3100CMPX	CMOS	6−Lead, 2x2 mm MLP	3,000 / Tape & Reel
FAN3100CSX	CMOS	5−Pin SOT23	3,000 / Tape & Reel
FAN3100TMPX	TTL	6−Lead, 2x2 mm MLP	3,000 / Tape & Reel
FAN3100TSX	TTL	5−Pin SOT23	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Table 2. RELATED PRODUCTS

Part Number	Type	Gate Drive (Note 12) (Sink/Src)	Input Threshold	Logic	Package
FAN3100T	**Single 2 A**	**+2.5 A/−1.8 A**	**TTL**	**Single Channel of Two−Input/One−Output**	**SOT23−5, MLP6**
FAN3100C	**Single 2 A**	**+2.5 A/−1.8A**	**CMOS**	**Single Channel of Two−Input/One−Output**	**SOT23−5, MLP6**
FAN3226C	Dual 2 A	+2.4 A/−1.6 A	CMOS	Dual Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3226T	Dual 2 A	+2.4 A/−1.6 A	TTL	Dual Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3227C	Dual 2 A	+2.4 A/−1.6 A	CMOS	Dual Non−Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3227T	Dual 2 A	+2.4 A/−1.6 A	TTL	Dual Non−Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3228C	Dual 2 A	+2.4 A/−1.6 A	CMOS	Dual Channels of Two−Input/One−Output, Pin Config. 1	SOIC8, MLP8
FAN3228T	Dual 2 A	+2.4 A/−1.6 A	TTL	Dual Channels of Two−Input/One−Output, Pin Config. 1	SOIC8, MLP8
FAN3229C	Dual 2 A	+2.4 A/−1.6 A	CMOS	Dual Channels of Two−Input/One−Output, Pin Config. 2	SOIC8, MLP8
FAN3229T	Dual 2 A	+2.4 A/−1.6 A	TTL	Dual Channels of Two−Input/One−Output, Pin Config. 2	SOIC8, MLP8
FAN3223C	Dual 4 A	+4.3 A/−2.8 A	CMOS	Dual Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3223T	Dual 4 A	+4.3 A/−2.8 A	TTL	Dual Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3224C	Dual 4 A	+4.3 A/−2.8 A	CMOS	Dual Non−Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3224T	Dual 4 A	+4.3 A/−2.8 A	TTL	Dual Non−Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3225C	Dual 4 A	+4.3 A/−2.8 A	CMOS	Dual Channels of Two−Input/One−Output	SOIC8, MLP8
FAN3225T	Dual 4 A	+4.3 A/−2.8 A	TTL	Dual Channels of Two−Input/One−Output	SOIC8, MLP8

12. Typical currents with OUT at 6 V and V_{DD} = 12 V.

WDFN6 2x2, 0.65P
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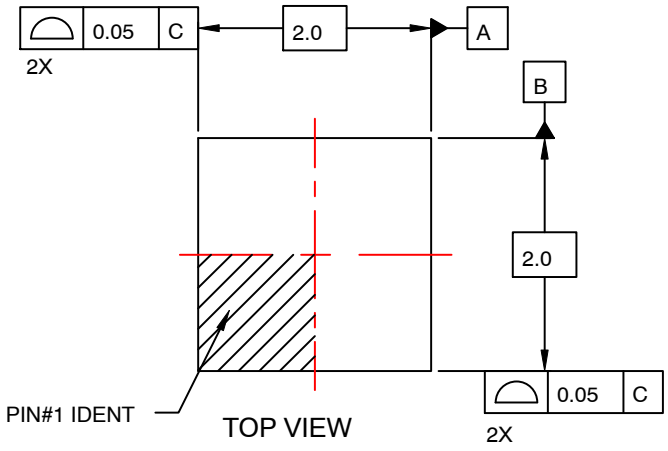
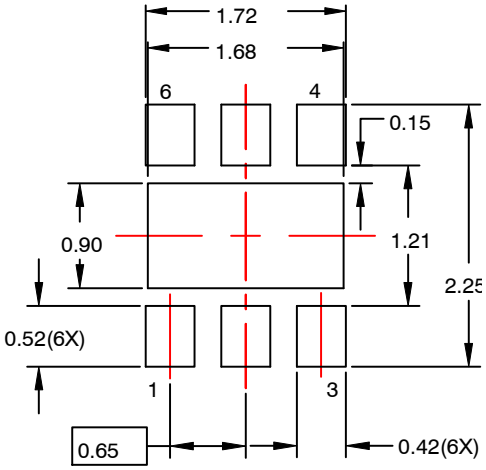
ISSUE O

DATE 31 JUL 2016





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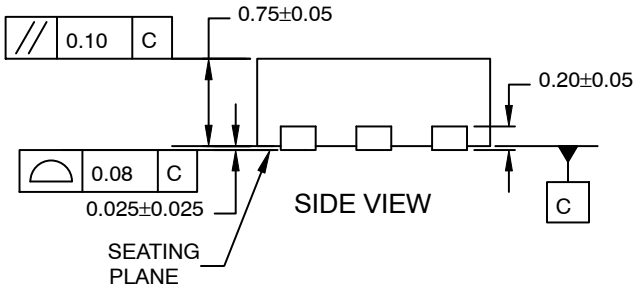

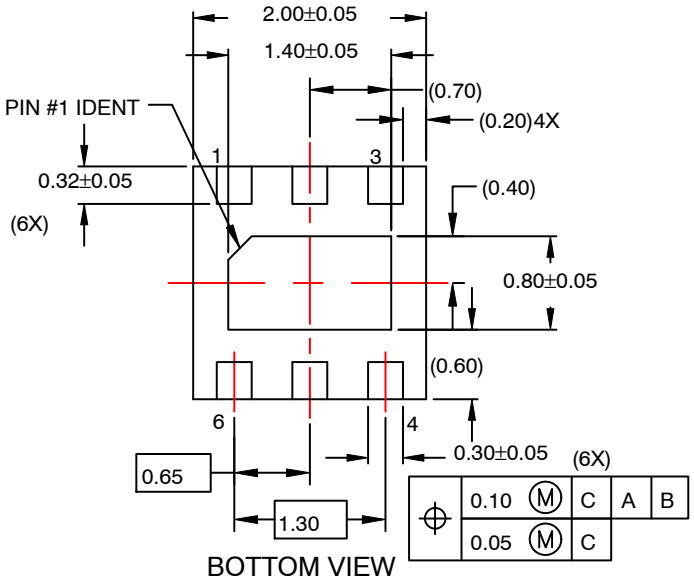

NOTES:

A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC MO−229 REGISTRATION

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

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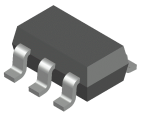

SOT−23, 5 Lead
CASE 527AH
ISSUE A

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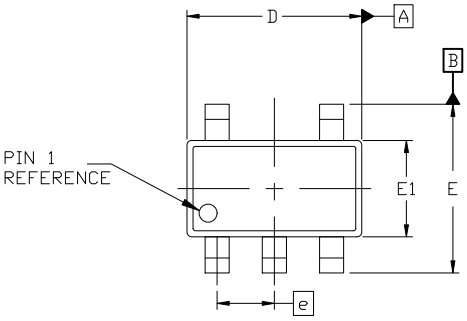
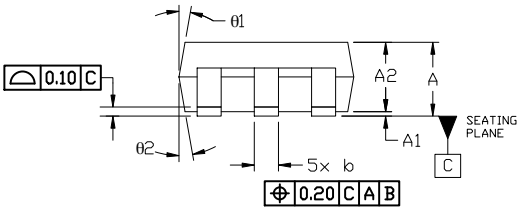
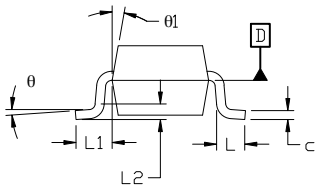


TOP VIEW



SIDE VIEW

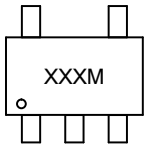


END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 19894
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.25 PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM D.
5. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL NOT BE LESS THAN 0.07mm.

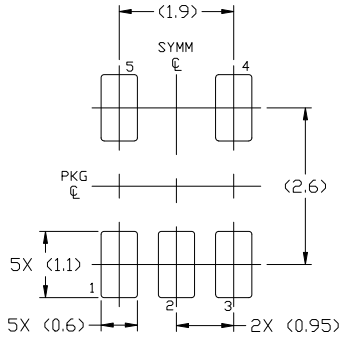
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	—	1.45
A1	0.00	—	0.15
A2	0.90	1.15	1.30
b	0.30	—	0.50
c	0.08	—	0.22
D	2.90 BSC		
E	2.80 BSC		
E1	1.60 BSC		
e	0.95 BSC		
L	0.30	0.45	0.60
L1	0.60 REF		
L2	0.25 REF		
θ	0°	4°	8°
θ1	0°	10°	15°
θ2	0°	10°	15°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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